SMPTE ST 2110 COMPLIANT SCALABLE ARCHITECTURE ON FPGA FOR END TO END UNCOMPRESSED PROFESSIONAL VIDEO TRANSPORT OVER IP NETWORKS

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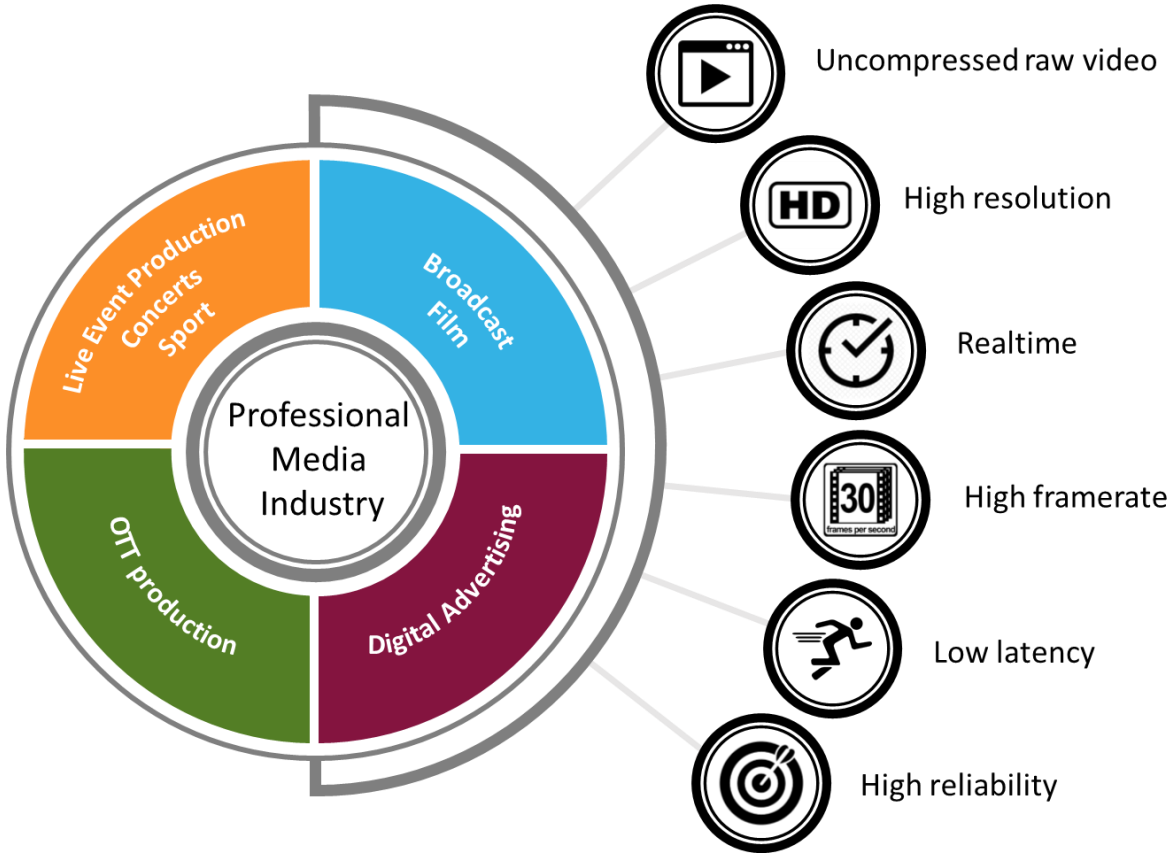
Professional Media Industry

- What is professional media industry?
- Currently uses SDI
- Trend to move into IP based networks
- Latest open standard for professional video over IP - SMPTE ST 2110



SMPTE ST 2110

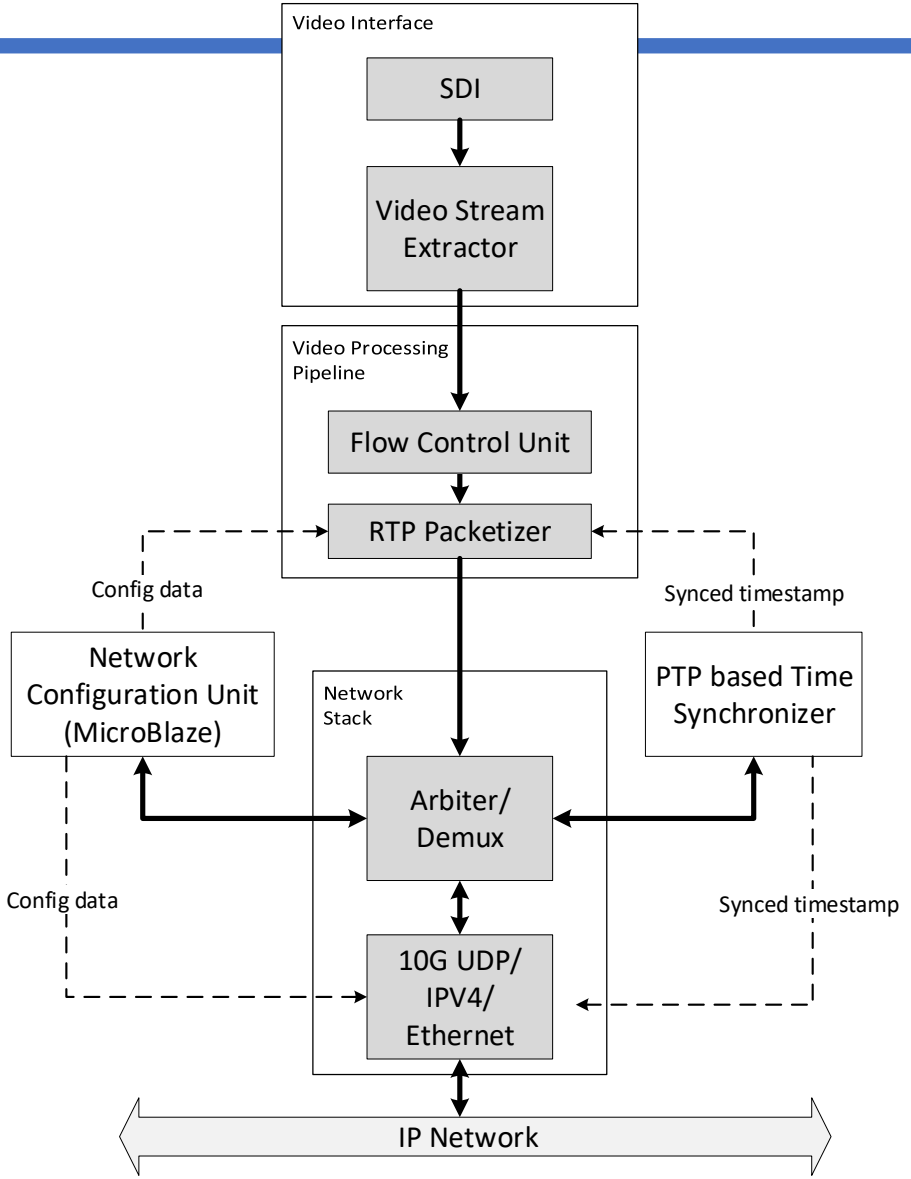
- Essence streams transmitted separately (audio, video, metadata)
- Can be implemented on software, but hardware implementations are more suitable

	Software	GPU	ASIC	FPGA
Jitter	High	Medium	Low	Low
Latency	High	Medium	Low	Low
Development time	Low	Medium/Low	High	Medium
Flexibility	High	Medium	Very low	Low
Cost for low volumes	Low	Medium	Very High	Medium/High

Our Proposal

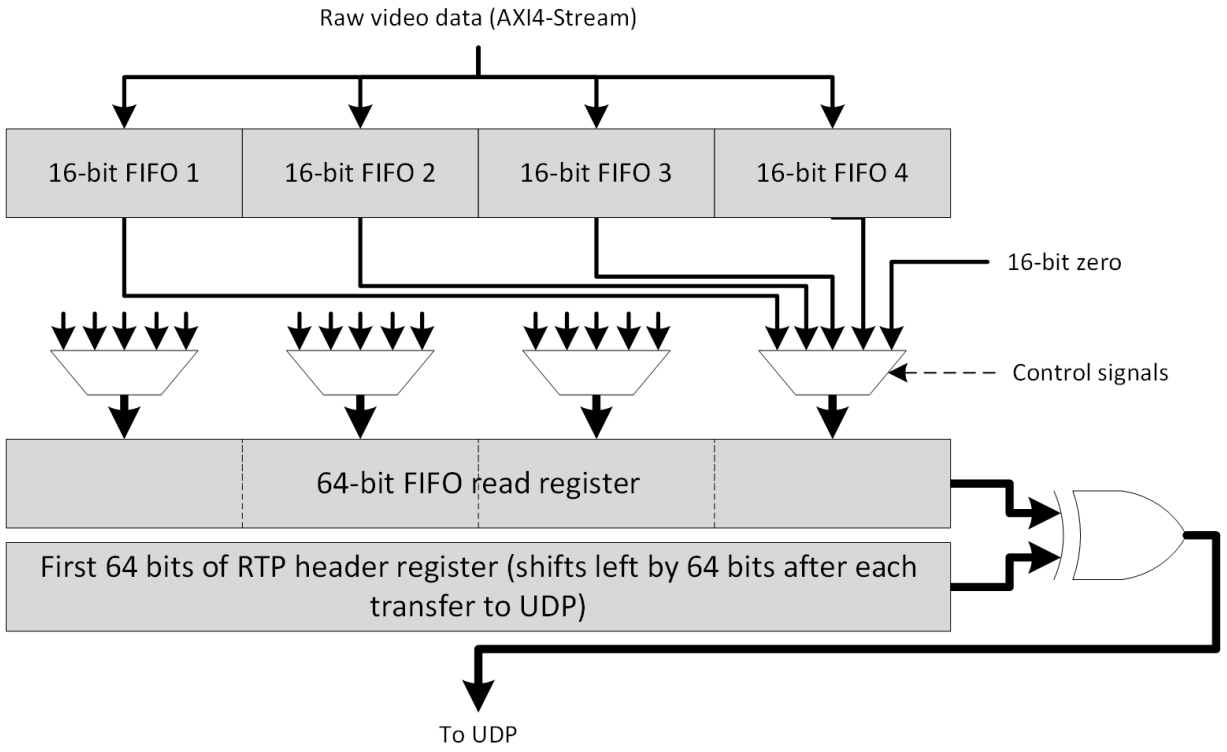
- A scalable hardware architecture for an FPGA based SMPTE ST 2110 compliant end to end solution.
- First such openly published architecture
- Low end to end latency
- High throughput

Hardware Architecture



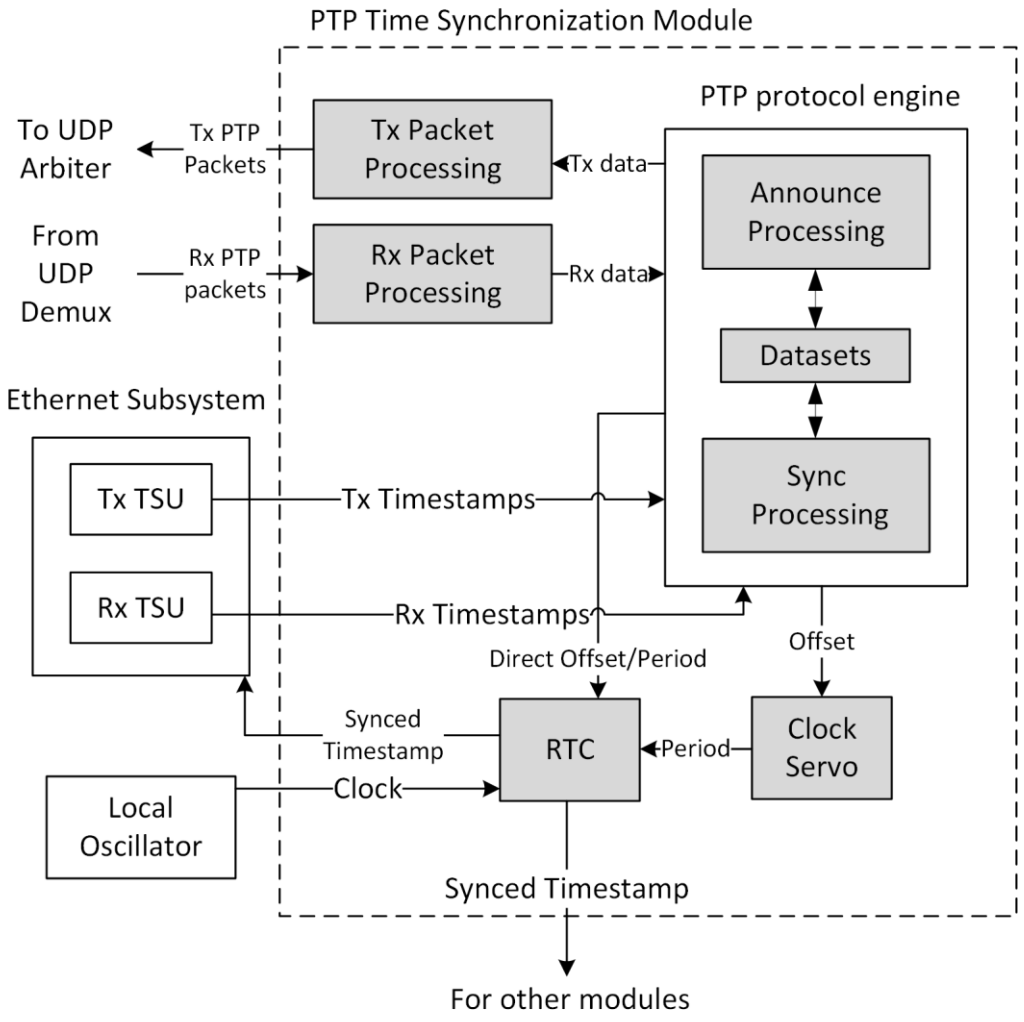
- Transmitter and receiver architectures are similar with the data flow direction reversed
- Four main groups
  1. Video interface
  2. Video processing pipeline
  3. Network stack
  4. Configuration/synchronization unit

Video Processing Pipeline



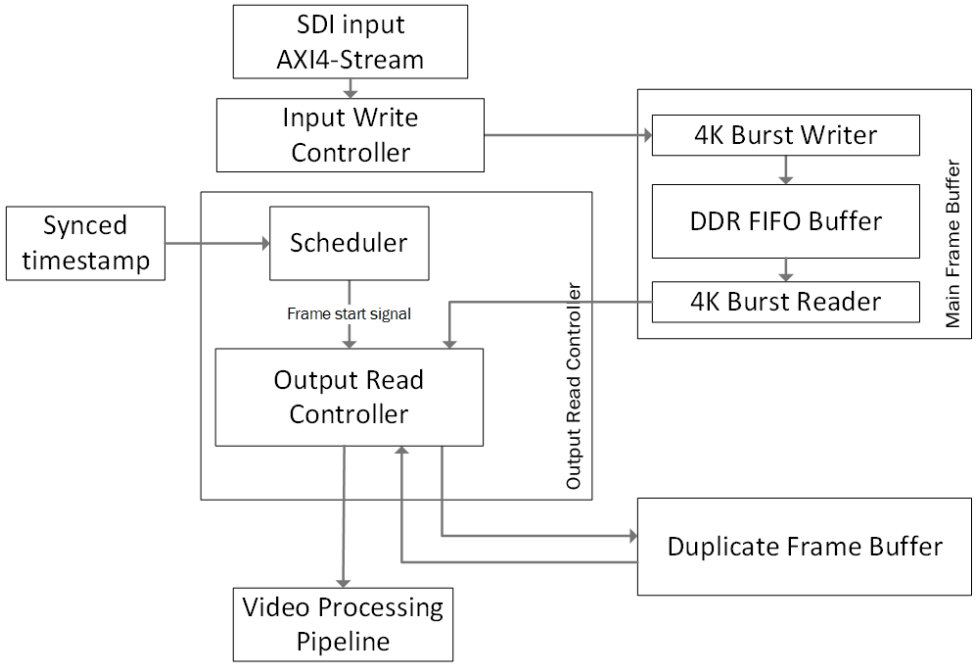
- RTP compliant
- Handles variable length headers at maximum throughput
- Pipelined architecture

PTP Hardware Level Timestamping



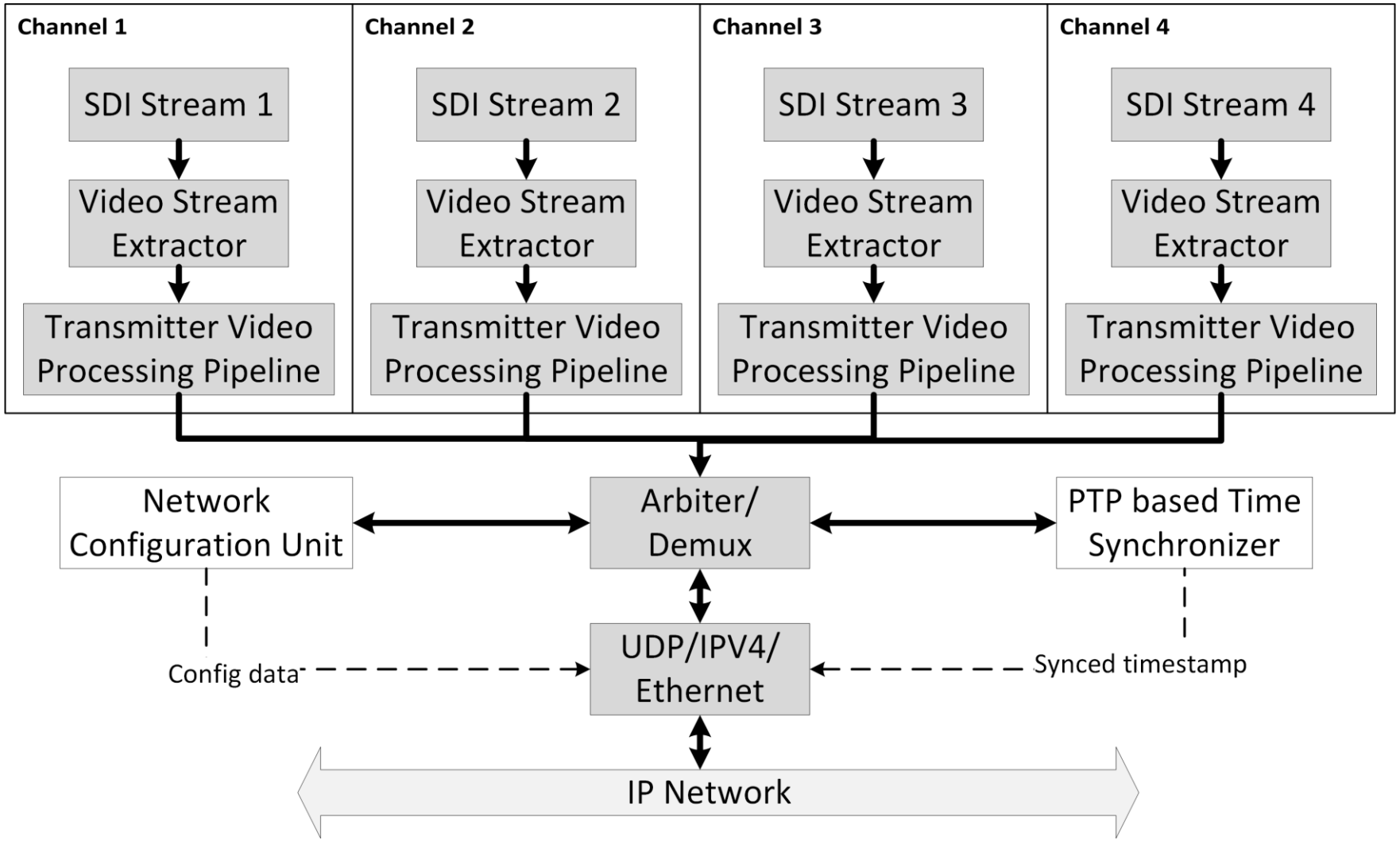
- Hardware timestamping at the XGMII interface
- Hardware design for higher accuracy and low synchronization time
- IEEE 1588 – 2008 v2 PTP standard along with ST 2059-1/2
- Workload distributed to submodules based on the functions performed

Flow Control and Traffic Shaping

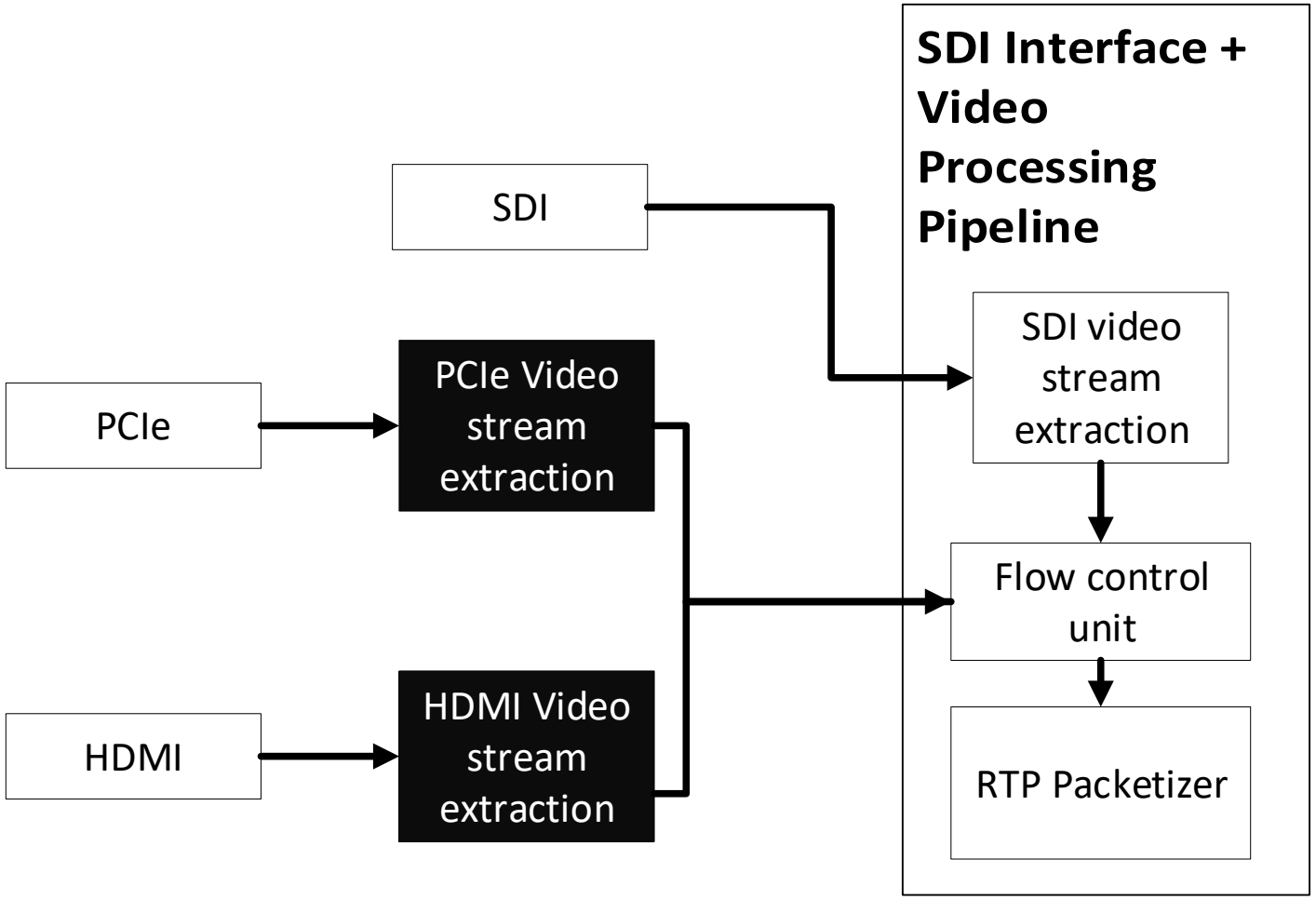


- Thresholding based flow controlling method
- Removes the effect of jitter in the network using buffers
- Traffic shaping follows a linear sender model as specified in ST 2110

Scalability



Interface Modularity



Results

- Max operating frequency – 200MHz
- Video processing pipeline – high throughput low latency packet processing
  - 4K 30fps at 100 MHz minimum frequency
- PTP time synchronization
  - Offset under 300ns at 62.5ms synchronization period
- Resource utilization - under 70K LUTs
- Latency max (end to end) - 8926 ns (mean – 8752ns)

Conclusion

- First openly published hardware architecture for SMPTE ST 2110
- Has potential for further improvements
  - Packet re-ordering module
  - End to end time synchronization (without dropping/ duplicating)
- Can be used as a baseline for future research based on ST 2110.

THANK YOU!