Event-Based Re-configurable Hierarchical Processors for Smart Image Sensors

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Motivation and Challenges

1. Continuous Increase in image size
2. Sequential operation
3. High power consumption
4. Application specific image sensor

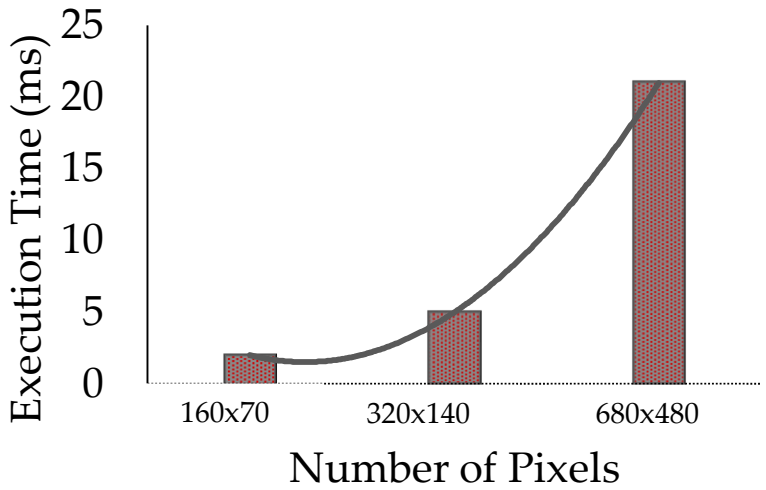

Figure 2: Increase of execution time with the increase of pixel counts

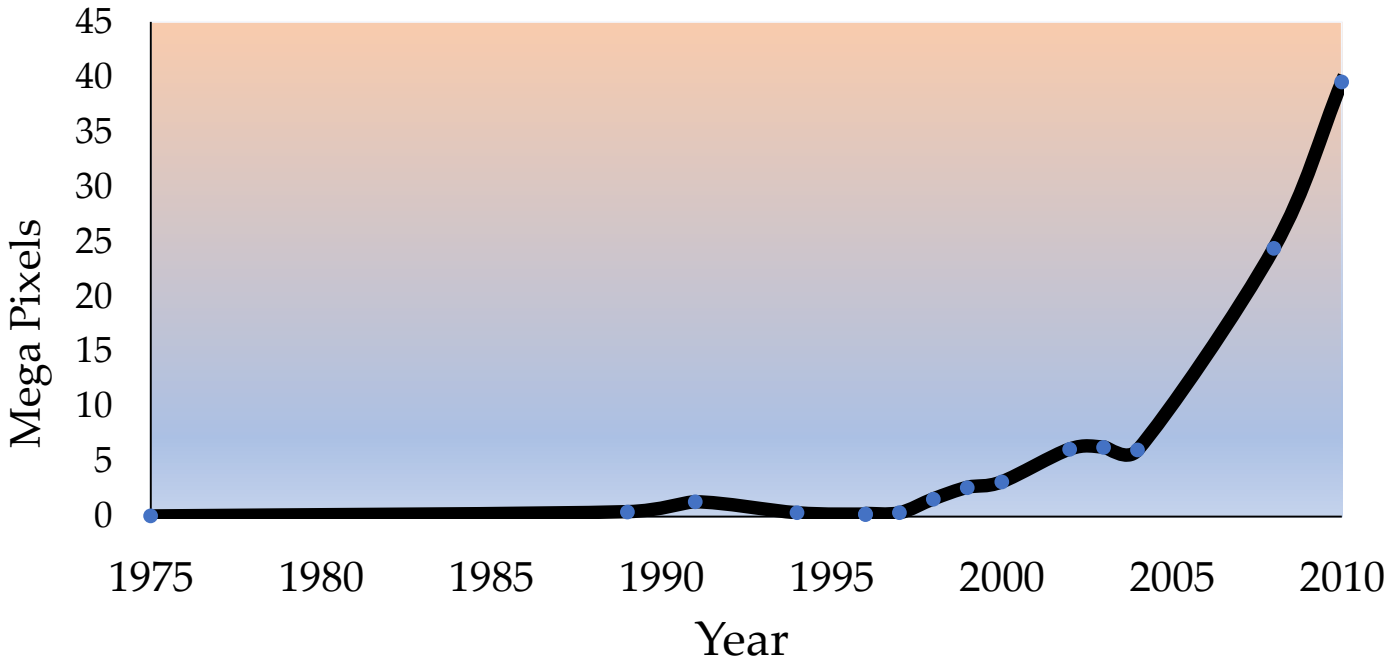

*Figure 1: Pixel Size Increase over the years in Digital Camera**

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*Source: https://www.macworld.com/article/1156514/35yearsofdigitalcameras.html

Viable Solutions

- Apply event-based processing instead of frame-based processing.
- Bringing the computational units close of the image sensor.
- Break sequential nature of image processing and introduce massive parallelism.
- Bio-Inspired computing promises to reduce power consumption.
- Hardware should be reconfigurable in ASIC paradigm.

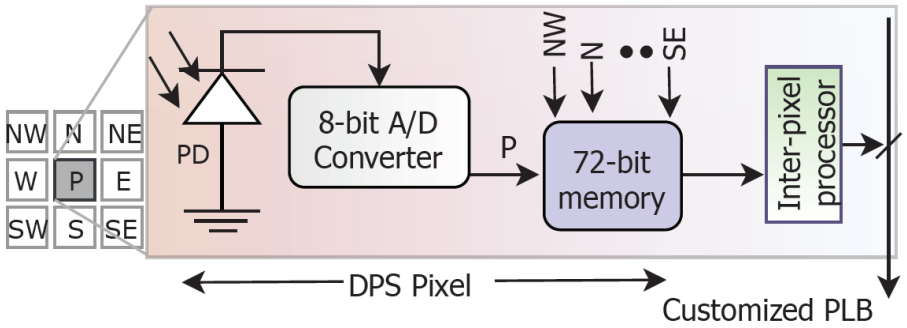

Figure 3: Pixel Circuit with computational unit

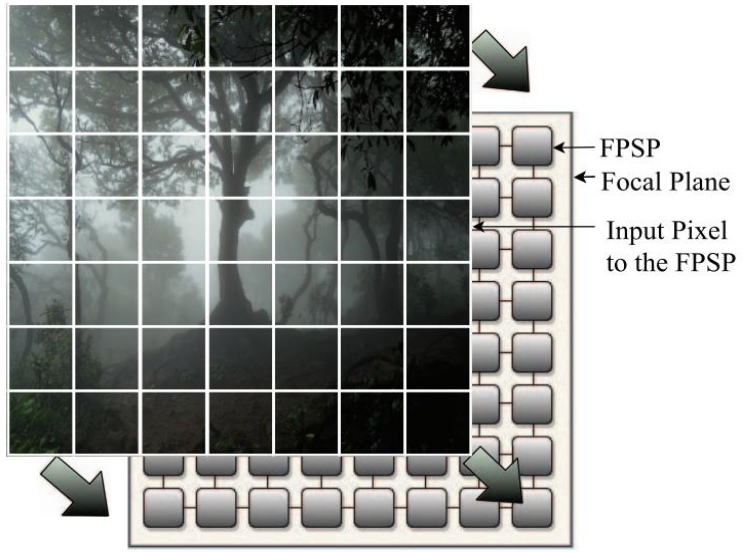

*Figure 4: Pixel-Parallel Focal Plane Image sensor where computational units are brought close to the image sensor**

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*Source: Bhowmik, Pankaj et al. "Design of a Reconfigurable 3D Pixel-Parallel Neuromorphic Architecture for Smart Image Sensor." *2018 IEEE/CVF Conference on Computer Vision and Pattern Recognition Workshops (CVPRW)* (2018): 786-7868.

Why Event-Based Processing is inevitable?

Frame Based Processing

Every Pixel is computed sequentially

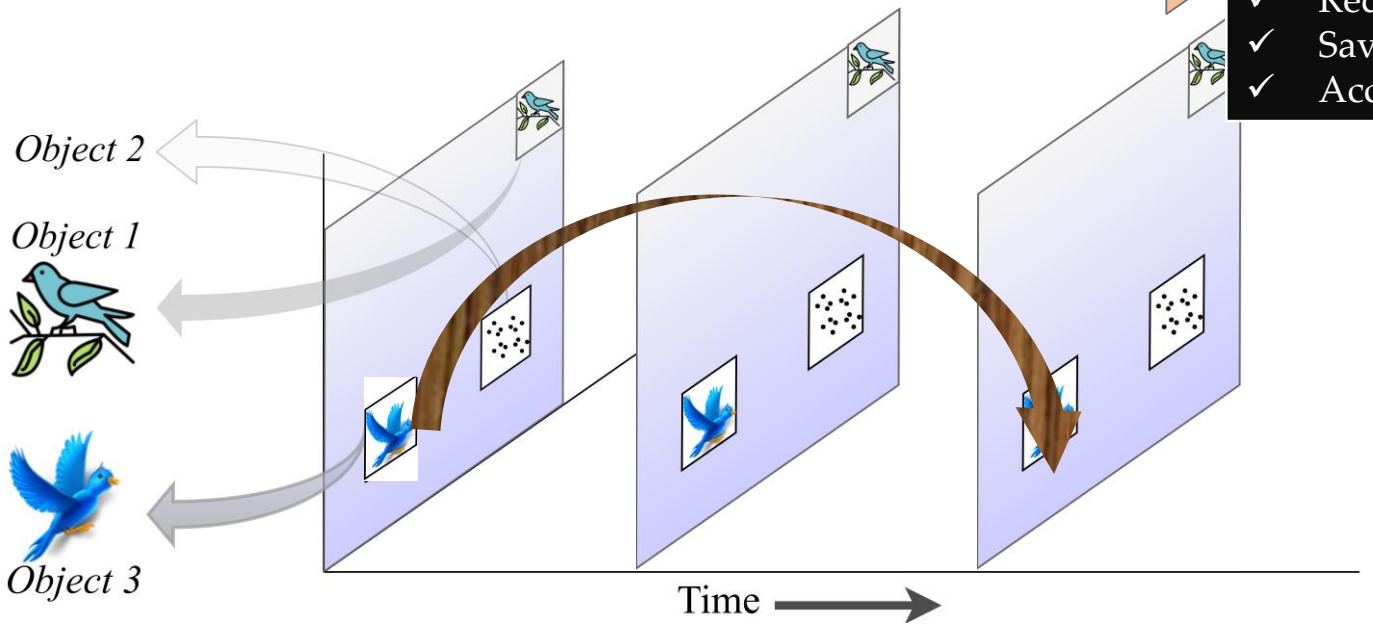
Event-Based Processing

Pixels with relevant information are computed in a sequential or parallel process

- ✓ Gleans effective information
- ✓ Reduces data volume
- ✓ Saves computational power
- ✓ Accelerate the processing

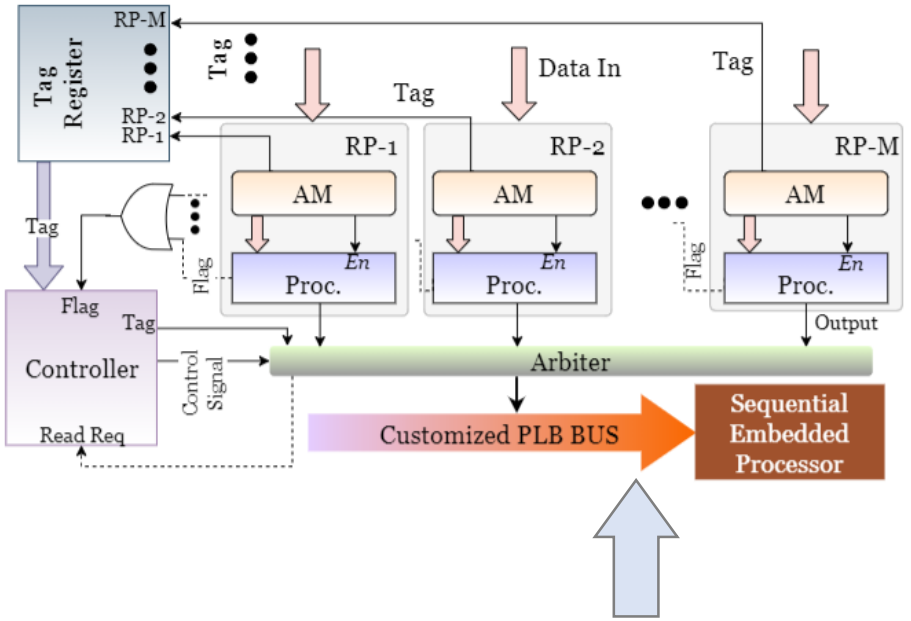
Convention Processing

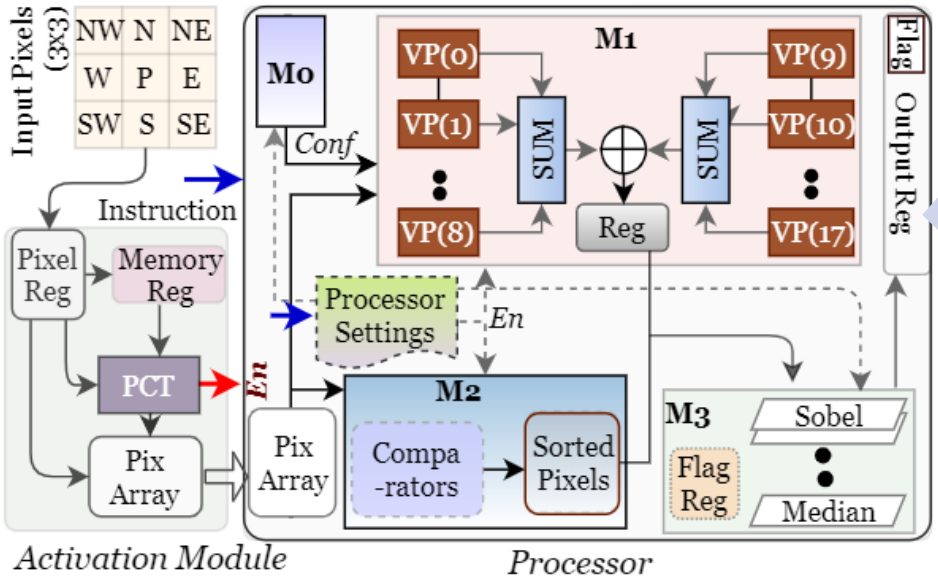
Event-Based Processing



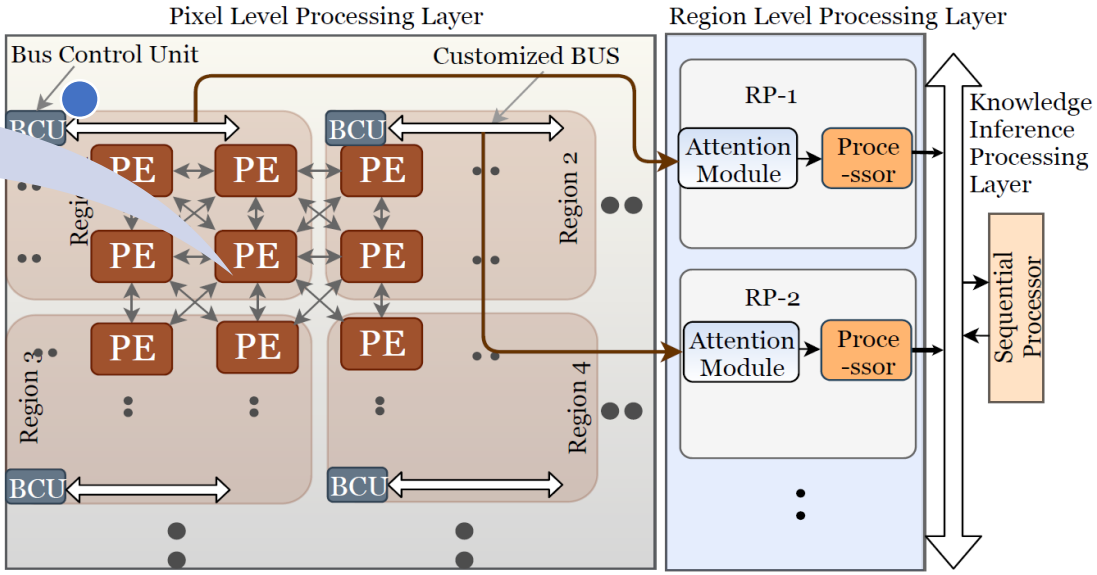
Proposed Architecture

1. Pixel-Level Processing Layer
2. Region-Level Processing Layer
3. Knowledge Inference Processing Layer





Single pixel circuit



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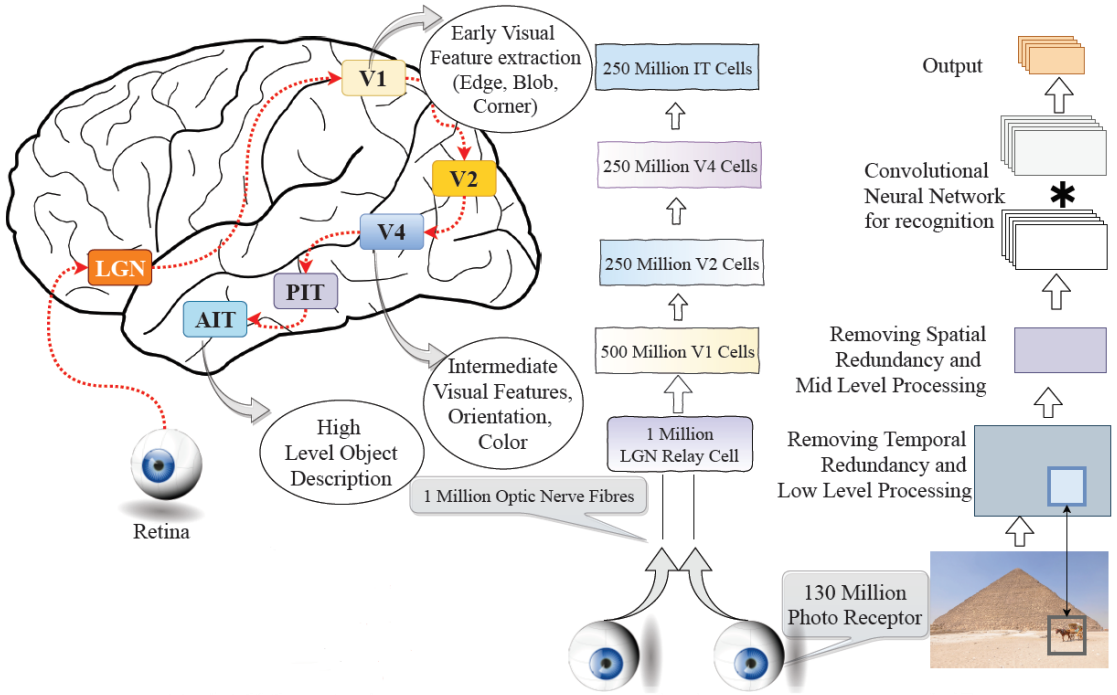
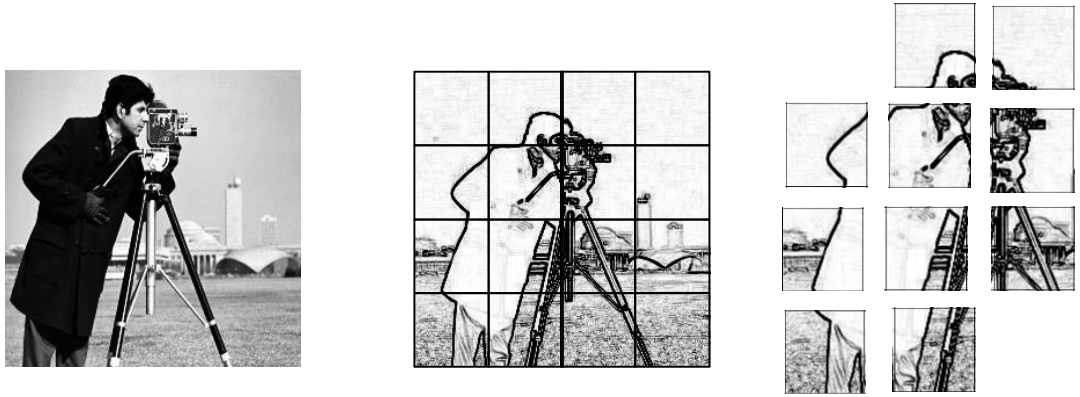
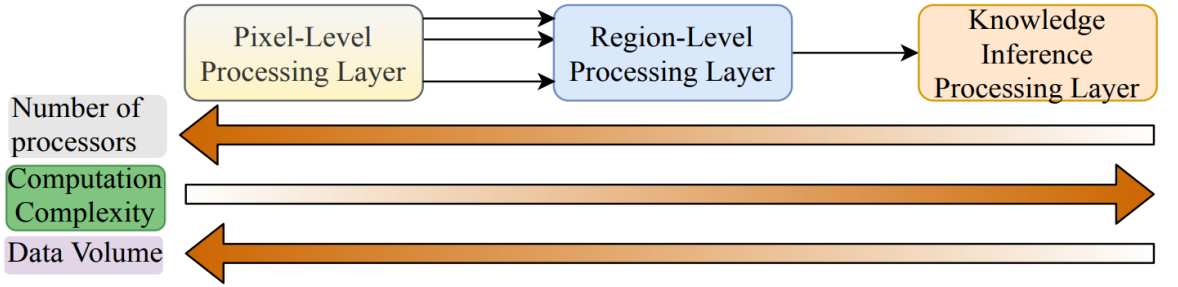
Hierarchical Processing

Biological Vision System is emulated in the proposed model







Functionality			
	1. Executes a set of low-level image processing 2. Removes temporal redundancy	*1. Executes a set of mid\high-level processing 2. Removes spatial redundancy*	*1. Employs Spatial Pyramid Pooling in CNN over variable set of input features to complete recognition*
	Sobel, Laplacian, Local Thresholding, Gaussian, Min filter, Median Filter, Max Filter and etc.	Blob detection, segmentation, corner detection, line detection, SIFT and etc.	Image reconstruction, clustering, matching for object recognition, high level reasoning.

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Pixel-Level Processing Layer

1. **Activation Module**: Predictive Coding in time

2. **Processor**: Reconfigurable to a set of Low-Level Image processing applications

   - M1 and M2 module executes the common section of the applications
   - M0 provides the convolutional kernel to the M1
   - M3 executes the unique segments
   - Processor setting block sets the configuration

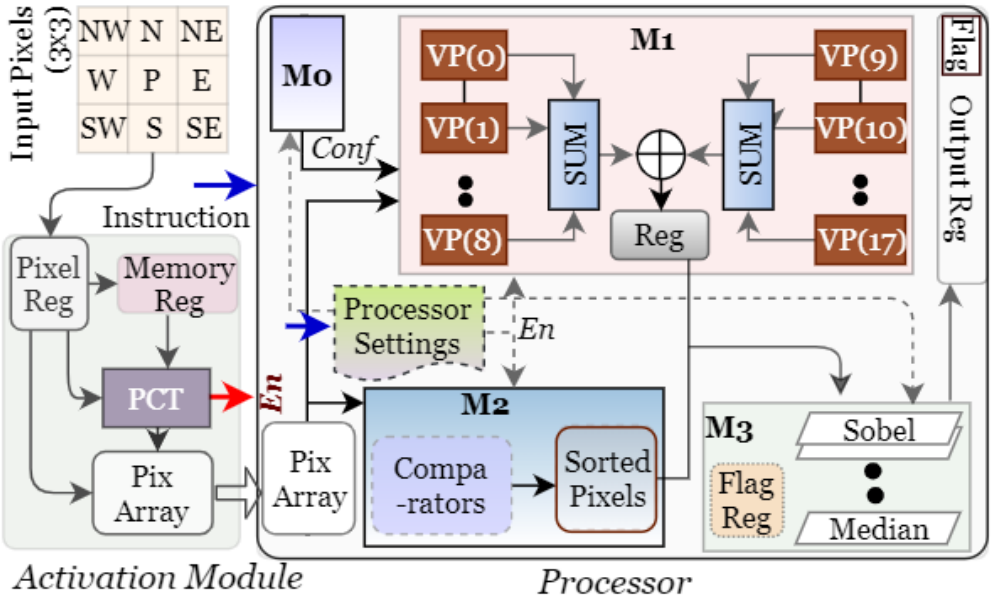
Inputs to the PE works with pixel ***P*** at time ***t-1***

NW	N	NE
W	**P**	E
SW	S	SE

PCT

Inputs to the PE works with pixel ***P*** at time ***t***

NW	N	NE
W	**P**	E
SW	S	SE



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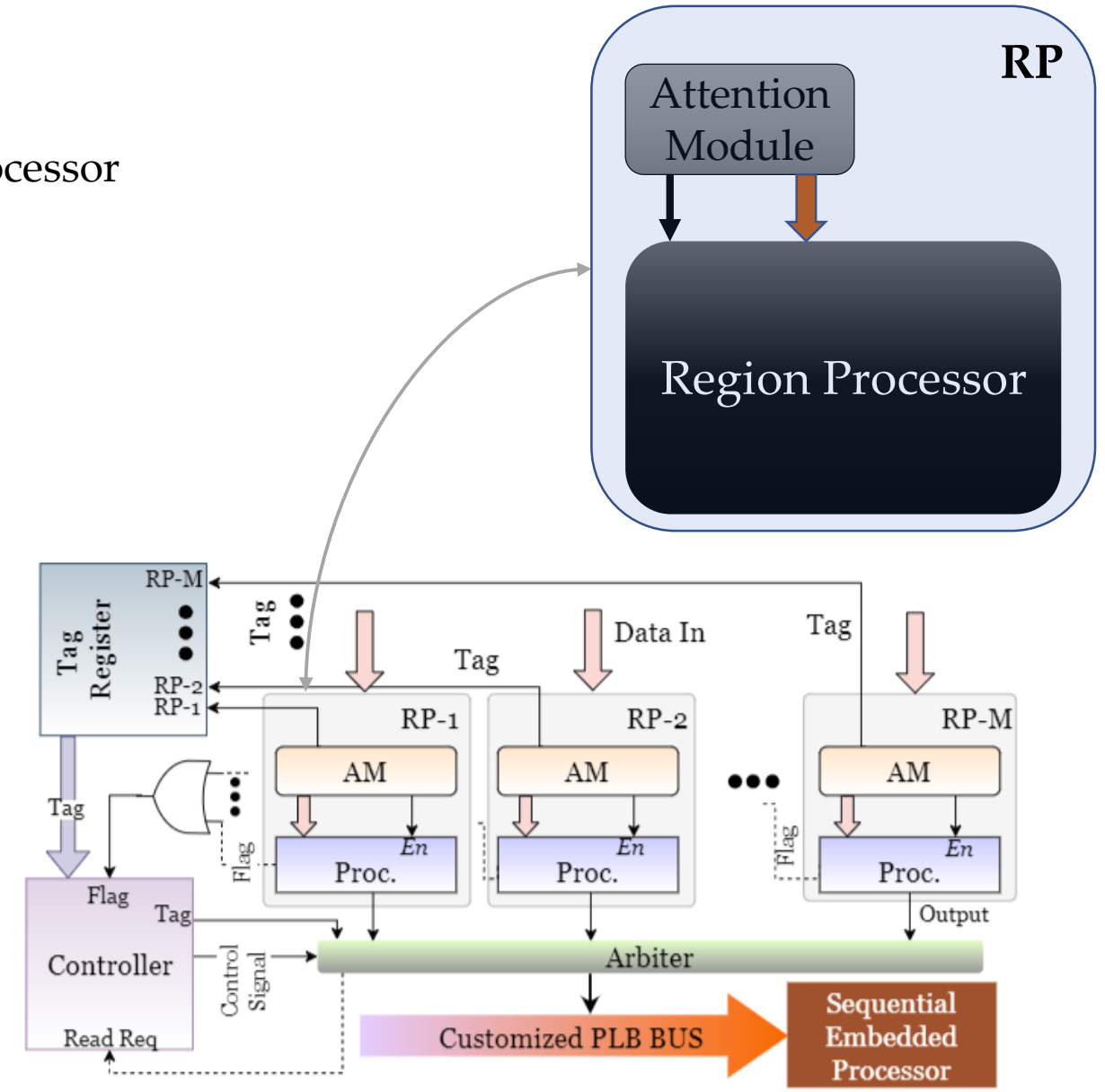
Region-Level Processing Layer

Attention Module (AM):

- ✓ Computes spatial saliency and activates the processor

Processor

- ✓ RP works on a larger region and provides region-level parallelism.
- ✓ Attention Module removes spatial redundancy.
- ✓ Region processors activates if there is an ROI.
- ✓ Arbiter sends global features to sequential processor from RP-1 to RP-M and only active RPs get the bus access.



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Knowledge Inference Processing Layer

- ✓ The external embedded processor receives reduces data from an image after removing temporal and spatial saliency.
- ✓ The received data it pre-processed by low-level and mid-level image processing operations.
- ✓ Hence the remainder operation in the machine vision task is less time consuming and computationally inexpensive.

Result Analysis: Pixel Level

- **Thirteen** low-level image processing applications are runtime reconfigurable.
- Predictive-Coding in Time removes temporal redundancy and gives **84.01% power savings**.
- The area and power overhead are in an acceptable range.
- The design achieves huge acceleration at the pixel level.

Table 1: Accurate prediction saves power from pixel level processors

	Prediction by the AcM		Without AcM
	Inaccurate	Accurate	
Power Consumption (mW)	4.884	0.781	4.1892
Dynamic Power Savings (%)	~	84.01	14.22
Execution Time (ns)	12.5	1.25	11.25
Speed up	~	10×	1.11×

Table 2: Execution Time comparison for executing low-level Applications

	Execution Time (ET)				
Image Size	CPU	Embedded Processor	GPU	FPGA	Our Implem -mentation
160x70	2 ms	28.74 ms	5.47 us	2 us	12.5 ns
320x140	5 ms	115.59 ms	5.50 us	4 us	12.5 ns
640x480	21 ms	791.07 ms	5.53 us	8 us	12.5 ns

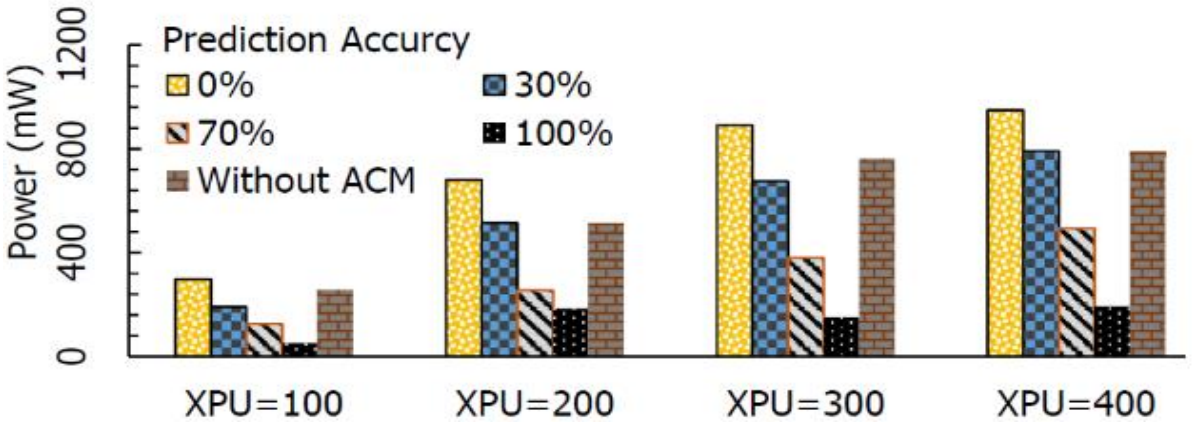

Figure: Possible power savings from different group of processing units (XPU)

Result Analysis: Region Level

RP performs the following operation on an 8x8 (*scalable*) region

- Region growing for segmentation
- Corner detection
- Scale Invariant Feature Detection (SIFT) for object recognition

Key Features

Runtime Reconfigurable for mid-level image processing applications
Saves **96.91%** power by dynamically postponing execution
Reduces data volume for sequential processor

Table 3: Parameter Extraction of the modules In ASIC

Module	Area (um2)	Power (mW)	Leakage (uW)	Delay (ns)
Attention Module	142.84	0.127	2.81	80
Proc.(Corner)	13830.67	11.46	333	93.75
Proc.(SIFT)	13804.86	11.43	331	146.25
Proc.(Seg)	886.3	3.938	43	160

Table 4: Parameter Extraction of the modules In FPGA

Module	Flip-Flop	LUT	No of clo -ck cycles	Power (mW)
Attention Module	422	168	64	15
Proc.(Corner)	768	1349	75	47
Proc.(SIFT)	1180	2323	117	128
Proc.(Segmentation)	661	1060	128	28

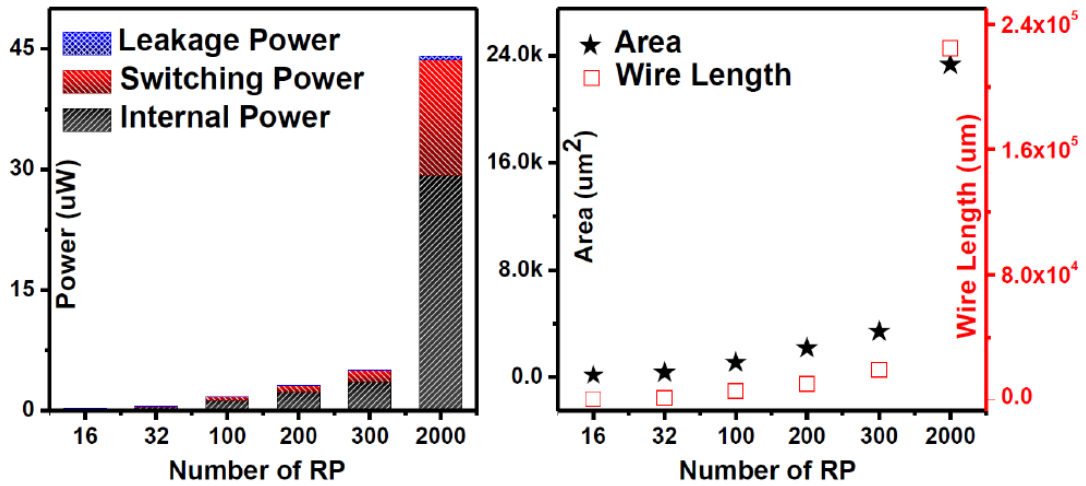

Figure: Increase in resource utilization for different number of PRs in the customized processor local BUS

Summary

- We prototype inter-pixel processor for an image sensor with hierarchical processing.
- Pixel-level processors execute low-level image processing applications after removing temporal redundancy.
- Region-level processors execute mid-level image processing applications after removing spatial redundancy.
- The gradual degradation of data volume accelerates the remainder task in a machine vision task on the sequential processor.
- Biological vision system is emulated on those processors to reduce power and speedup the system.
- The processors are implemented on hardware (ASIC and FPGA) and they are runtime reconfigurable to ensure a flexible design after fabrication.

Thank You

for

Your Concentration

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