ASAP'19 – (July 15-17)

Bank-selective Strategy for Gate-based Ternary Content-addressable Memory on FPGAs

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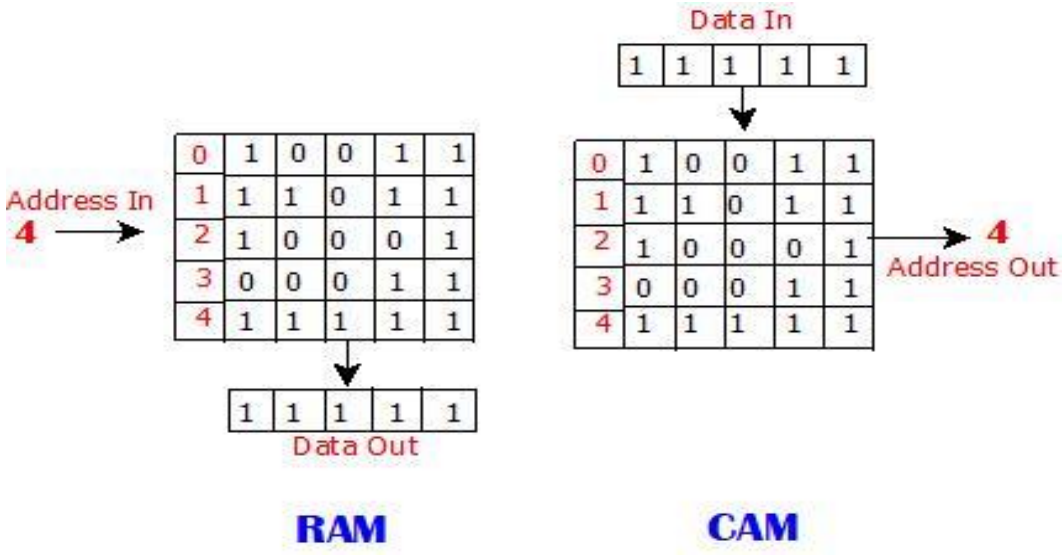
Paper# 57

RAM vs. CAM

- Random-access Memory (RAM):
  - Returns data at the given search address.
  - It takes many clock cycles to find the address of a specific data.



- Content Addressable Memory (CAM):
  - Returns address of the given search input.
  - It takes only one clock cycle to find the address of a specific data.

Applications

- Security Systems
- Network Routers

Table 1: 4 to 2 Encoder

Input				Output		Decimal
1	0	0	0	0	0	0
0	1	0	0	0	1	1
0	0	1	0	1	0	2
0	0	0	1	1	1	3

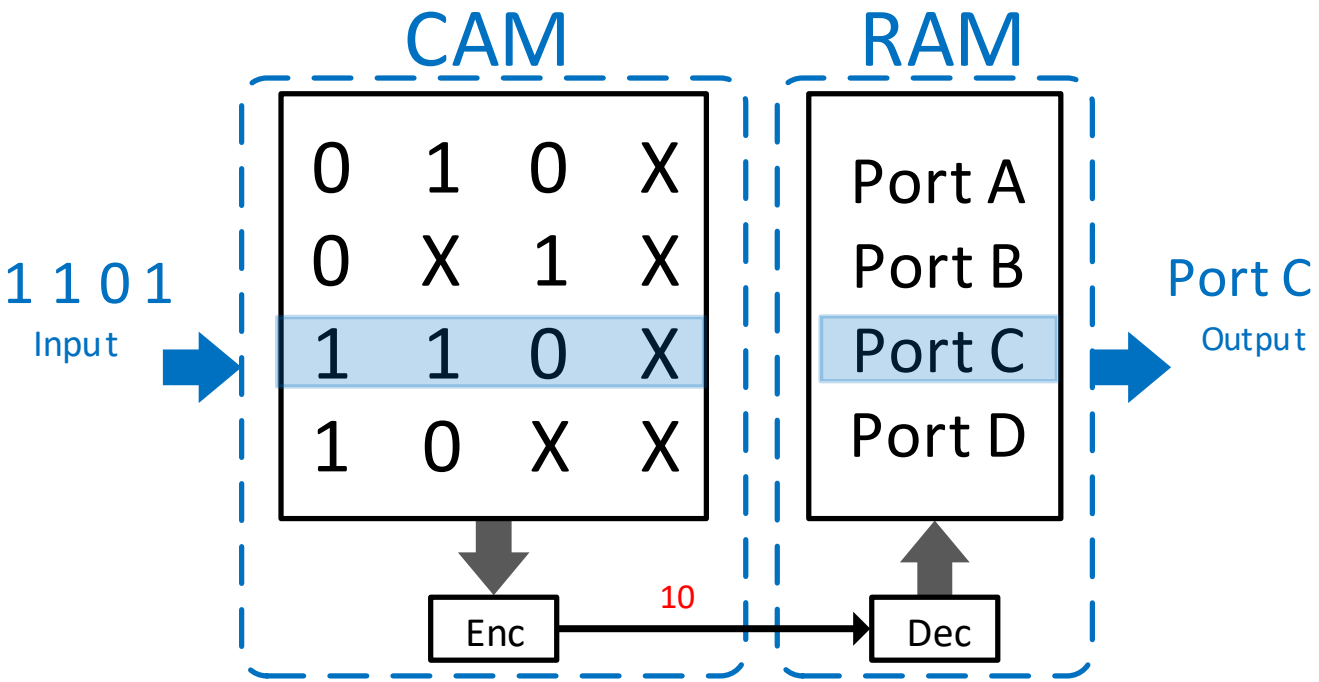


Fig. 3: Network Router using CAM and RAM

Problem Definition

- No hard IP in modern FPGAs
  - Xilinx presented a soft IP in 2017 for SDNet.

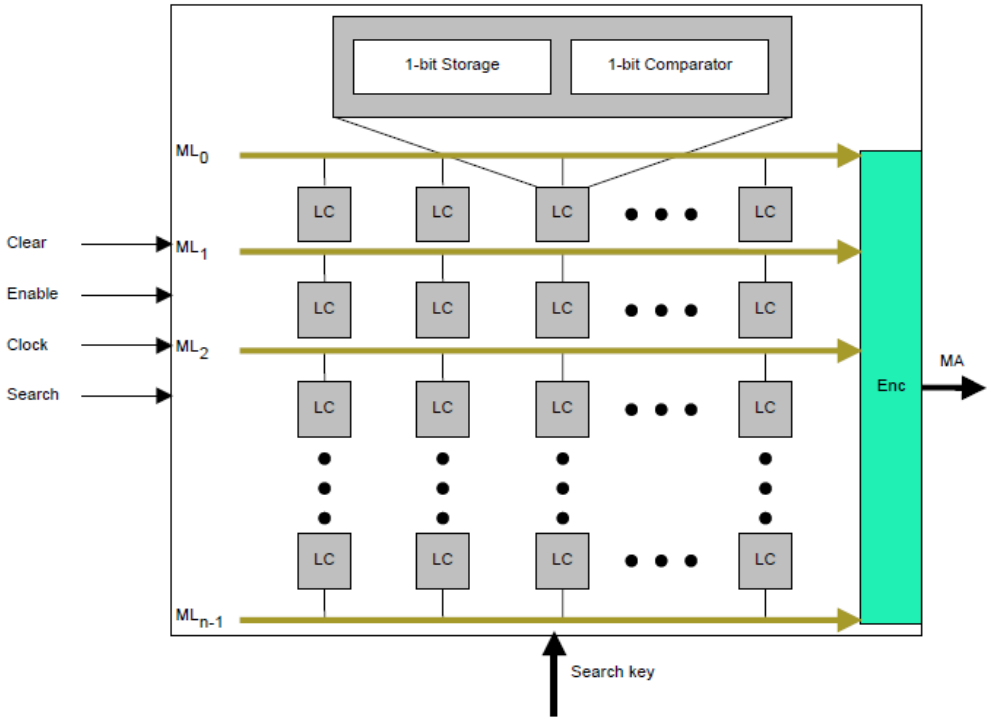
- Why not to make RAM function like CAM
  - Try to use the least number of RAM cells to emulate CAM

  - FPGAs are enriched with RAM cells, flip-flops etc. So to use these blocks to emulate CAM.
    - Power Consumption
    - Speed
    - Hardware Resources

LH-CAM

- Logic based Higher Performance Binary CAM
- Implemented 64 x 36 LH-CAM on Xilinx Virtex-6 FPGA.
  - One flip-flop per BCAM bit

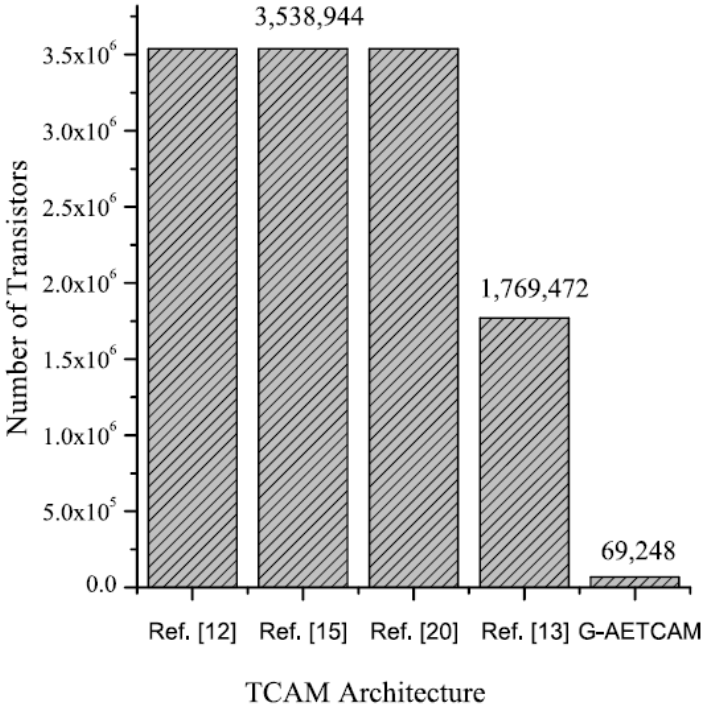
- It showed improvement in
  - Speed,
  - Power Consumption,
  - Logical Resources

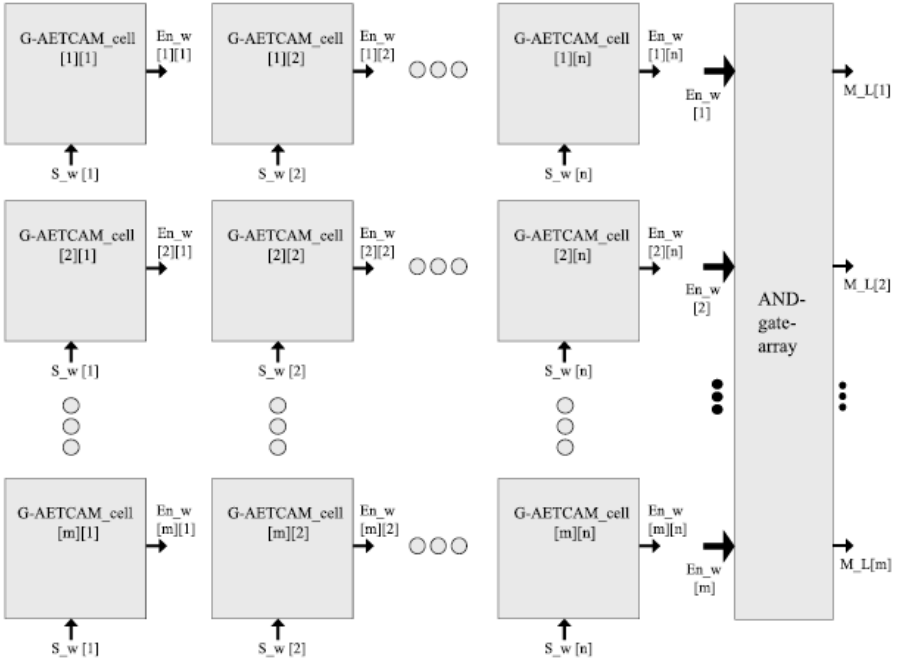


Ullah, Zahid. "LH-CAM: Logic-based higher performance binary CAM architecture on FPGA." *IEEE Embedded Systems Letters* (2017)

G-AETCAM

- Gate based Area Efficient Ternary content addressable Memory
  - Two flip flops per TCAM bit
- Implemented 64 x 36 G-AETCAM on Xilinx Virtex-6 FPGA.



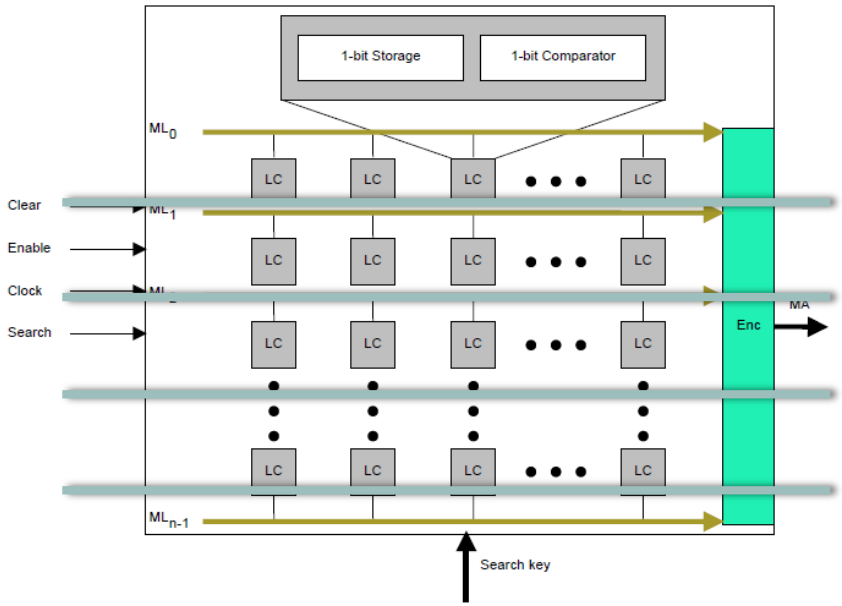


Irfan et. al. "G-AETCAM: Gate-based area-efficient ternary content-addressable memory on FPGA." *IEEE Access* (2017)

Proposed Work

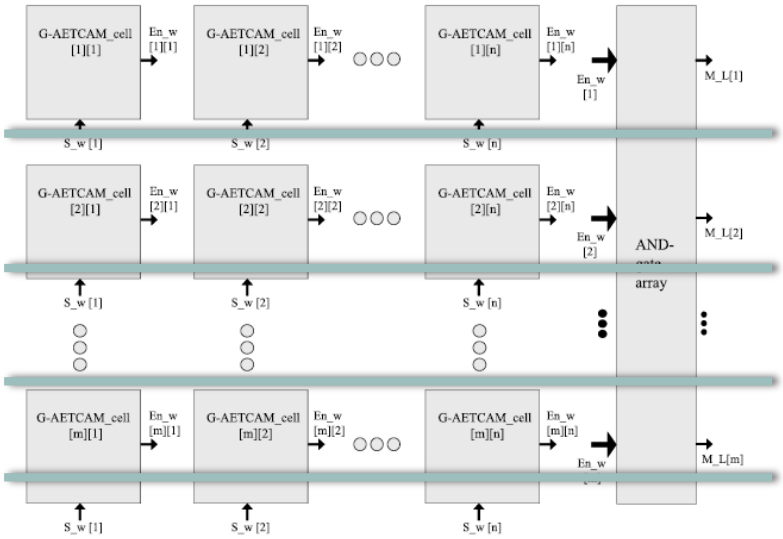
- Bank Selective Strategy for Gate-based CAM
  - Divide in 4 banks – Theoretically 75% Power reduces

Binary CAM [6]



42 % Reduction

Ternary CAM [1]



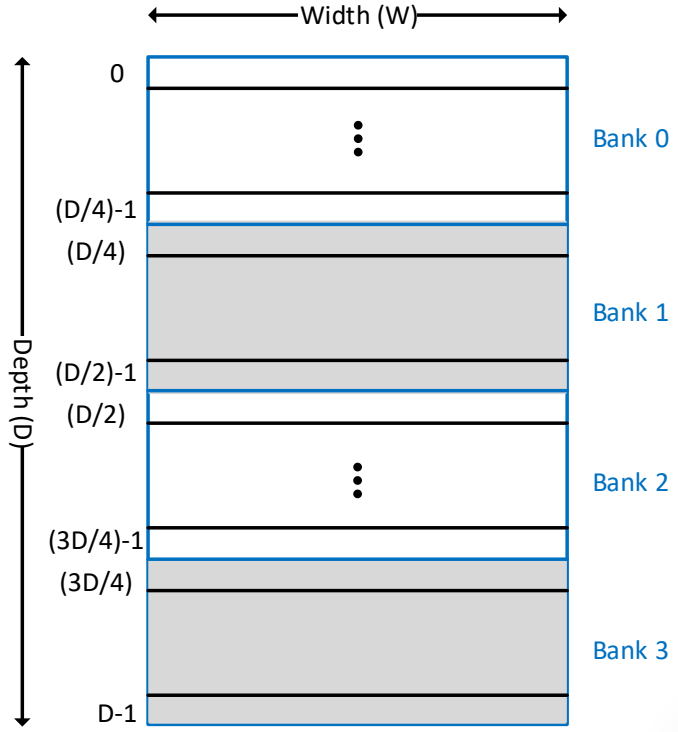
48 % Reduction

Power Consumption

Conclusion and Future Work

- Initial evaluation shows the feasibility of the idea on gate-based TCAM.
- What if we increase the number of banks?
  - 8 banks instead of 4?
- Upcoming Work
  - The position of selector-bits
  - Bank overflow
  - Merge the use of lookup tables and FFs

Sw [w-1:w-2]	Bank for Searching
0 0	Bank 0
0 1	Bank 1
1 0	Bank 2
1 1	Bank 3



References

- [1] Irfan, Muhammad, and Zahid Ullah. "G-AETCAM: Gate-based area-efficient ternary content-addressable memory on FPGA." *IEEE Access* 5 (2017): 20785-20790.
- [2] Somasundaram, Madian. "Circuits to generate a sequential index for an input number in a pre-defined list of numbers." U.S. Patent No. 7,155,563. 26 Dec. 2006.
- [3] Ullah, Zahid, Kim Ilgon, and Sanghyeon Baeg. "Hybrid partitioned SRAM-based ternary content addressable memory." *IEEE Transactions on Circuits and Systems I: Regular Papers* 59.12 (2012): 2969-2979.
- [4] Jiang, Weirong. "Scalable ternary content addressable memory implementation using FPGAs." *Proceedings of the ninth ACM/IEEE symposium on Architectures for networking and communications systems*. IEEE Press, 2013.
- [5] Ahmed, Ali, Kyungbae Park, and Sanghyeon Baeg. "Resource-efficient SRAM-based ternary content addressable memory." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 25.4 (2017): 1583-1587.
- [6] Ullah, Zahid. "LH-CAM: Logic-based higher performance binary CAM architecture on FPGA." *IEEE Embedded Syst. Lett.* 9.2 (2017): 29-32.
- [7] Hassan, et al. "Beyond the Limits of Typical Strategies: Resources Efficient FPGA-based TCAM." *IEEE Embedded Systems Letters* (2018).

Thank you for your attention ☺

- Additional slides

FPGA based TCAMs

- RAM based TCAMs [3, 5]
  - HP-TCAM, Z-TCAM, E-TCAM
    - Partitioned to fit 512x36 into FPGA BRAMs

- Logic based CAMs
  - LH-CAM (binary CAM)
  - G-AETCAM (ternary CAM)
    - The optimization parameters are:
      - Speed
      - Power
      - Hardware Resources

Ullah et al. “Hybrid partitioned SRAM-based ternary content addressable memory." *IEEE Transactions on Circuits and Systems I: Regular Papers* (2012)

Classification

- On the basis of the storing bits, CAM can be classified as:
  - Binary CAM
  - Ternary CAM

    - Binary CAM (BiCAM)
      - Simplest Type of CAM
      - Stores only binary words (1s and 0s)

    - Ternary CAM (TCAM)
      - In addition to 1s and 0s it supports a third state "**X**".
      - **X** is known as the don't care state
      - For instance a TCAM word of 10X1 may match to 1001 or 1011.

Conclusion and Future Work

- Initial evaluation shows the feasibility of the idea on gate-based TCAM.
- Problems:
  - Bank Selection saves power but the memory capacity shrinks.
  - Scalability
  - Bank Overflow
- Future Work:
  - Find the optimal number of banks
  - Solution for the bank overflow

FPGAs

- Field Programmable Gate Arrays
  - Reconfigurable Hardwares
- Hardware Description Language
  - Verilog
  - VHDL
- Synthesizer
  - Code to Hardware translator

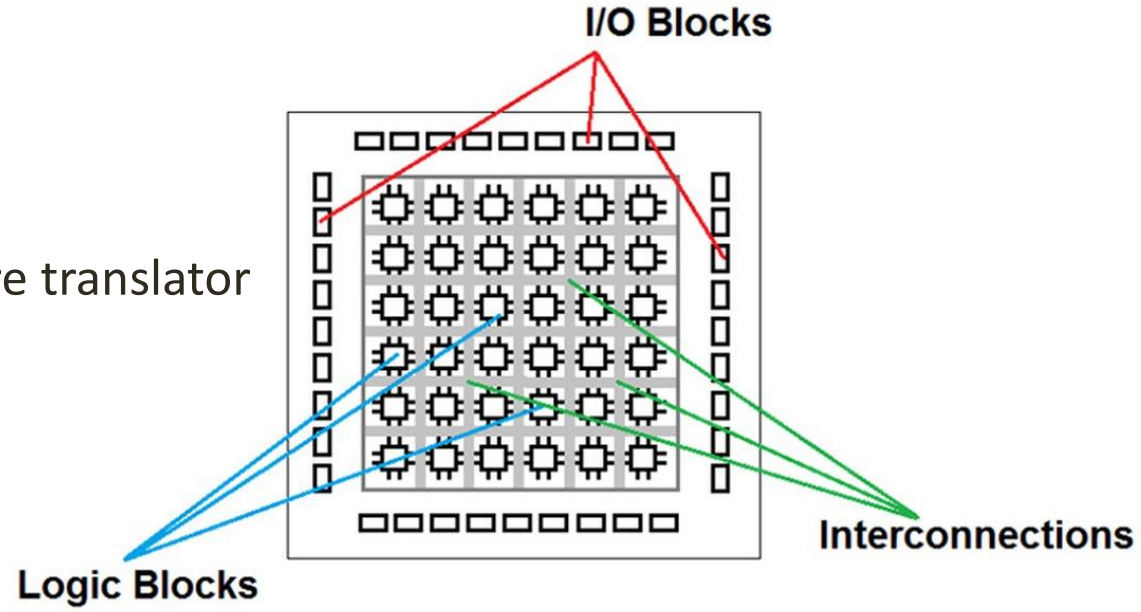
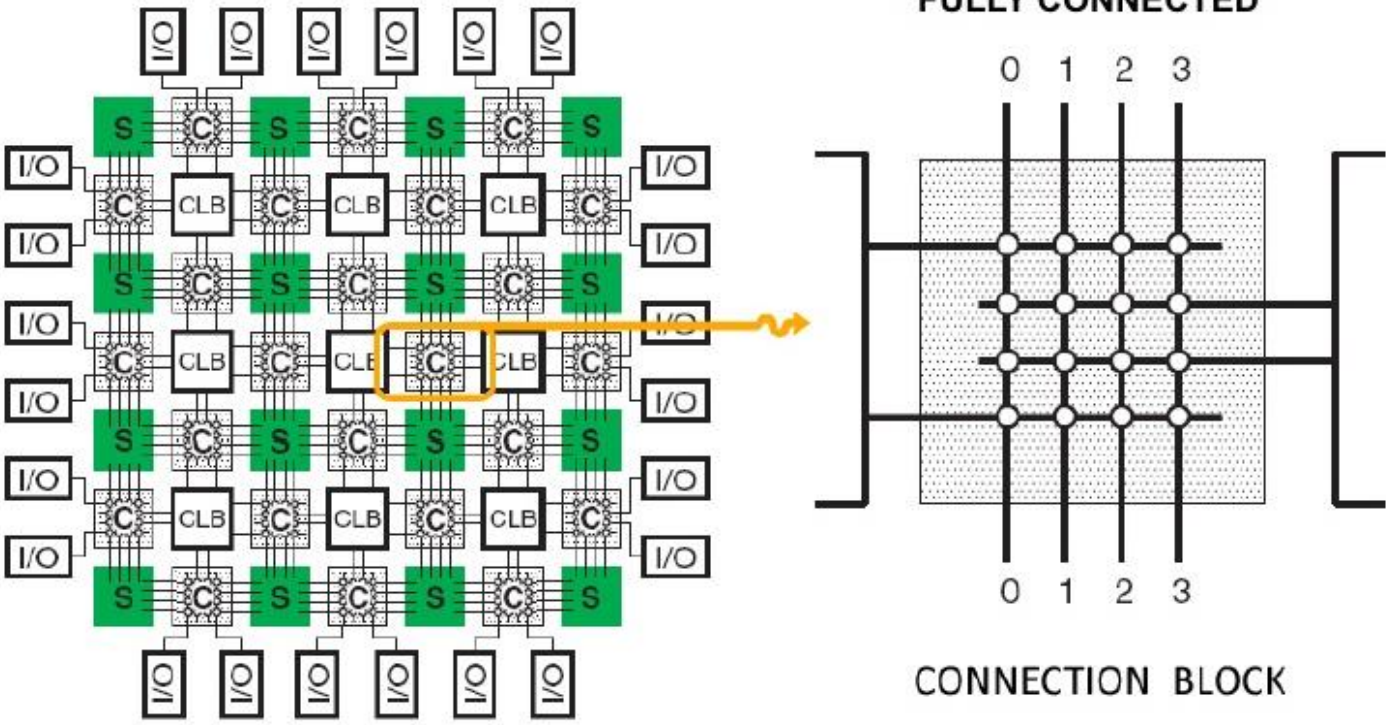


Fig. 2: Basic Structure of an FPGA


I/O
S
C
CLB
"FULLY CONNECTED"
0 1 2 3
0 1 2 3
CONNECTION BLOCK