ESRG
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Application Specific Architecture for Hardware Accelerating HOG-SVM to Achieve High Throughput on HD Frames

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COMPETE
QREN Quadro de Referência Estratégico Nacional
União Europeia Fundo Europeu de Desenvolvimento Regional
FCT Fundação para a Ciência e a Tecnologia
Ministério da Ciência, Tecnologia e Ensino Superior

Topics

- Introduction
- Background
- Architecture and Methodology
- Results
- Conclusion

Introduction

- Computer Vision is an emerging field with diverse applications which encompasses many algorithms with heavy computations.

Introduction

- Histogram of Oriented Gradients-Support Vector Machine (HOG-SVM) is one such versatile algorithm used for object detection and image classification despite it's heavy computation load.

Introduction

- Processing such an algorithm in real time with adequate throughput is a challenging task for a general purpose processor.

Introduction

- Moreover, an embedded CPU with very limited processing power could least cater such heavy processing.

Introduction

- Therefore our research in general focuses on developing application specific architectures for hardware acceleration of computer vision algorithms.

Introduction

- This paper presents a continuation of a series of research to hardware accelerate HOG-SVM algorithm on FPGA.

Introduction

- In this paper we mainly present the high performance application specific architecture for hardware acceleration of HOG-SVM which was successful in achieving a high throughput of 240fps on HD frames of size 1920x1080 which is a significant improvement of performance compared to previous research.

Introduction

- On the other hand, both hardware utilization and power consumption are minimized

Introduction

- A mechanism based around Block RAM (BRAM) structures and deep pipelining are used as the key architectural techniques of achieving high performance.

Introduction

- The proposed design was deployed on Zynq7000 FPGA platform which contains a hardwired ARM CPU along with the programmable FPGA fabric

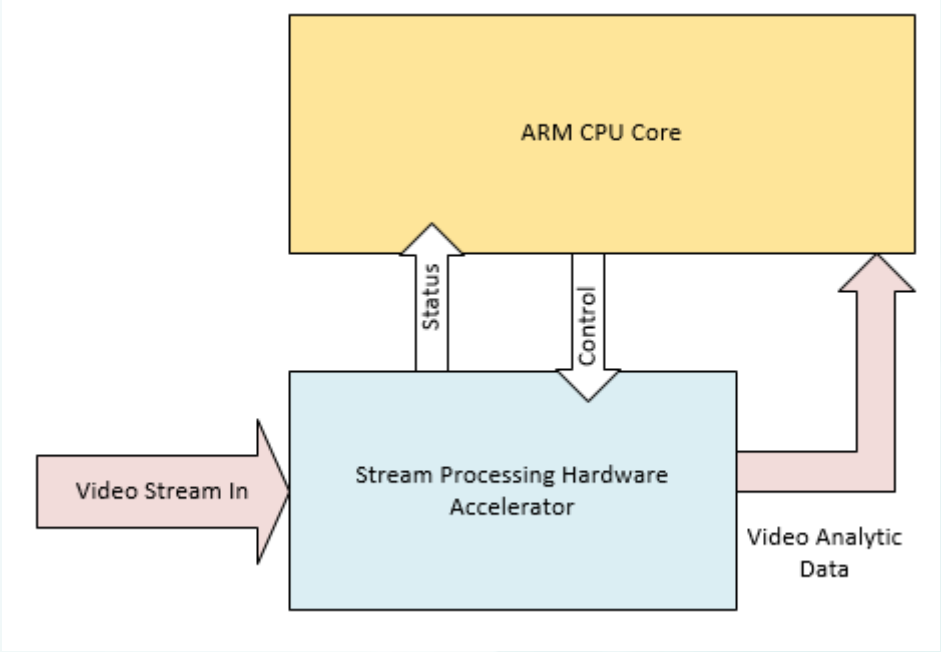
Introduction

- The accelerator is deployed on the FPGA and integrated with the ARM CPU using AXI memory interfaces.

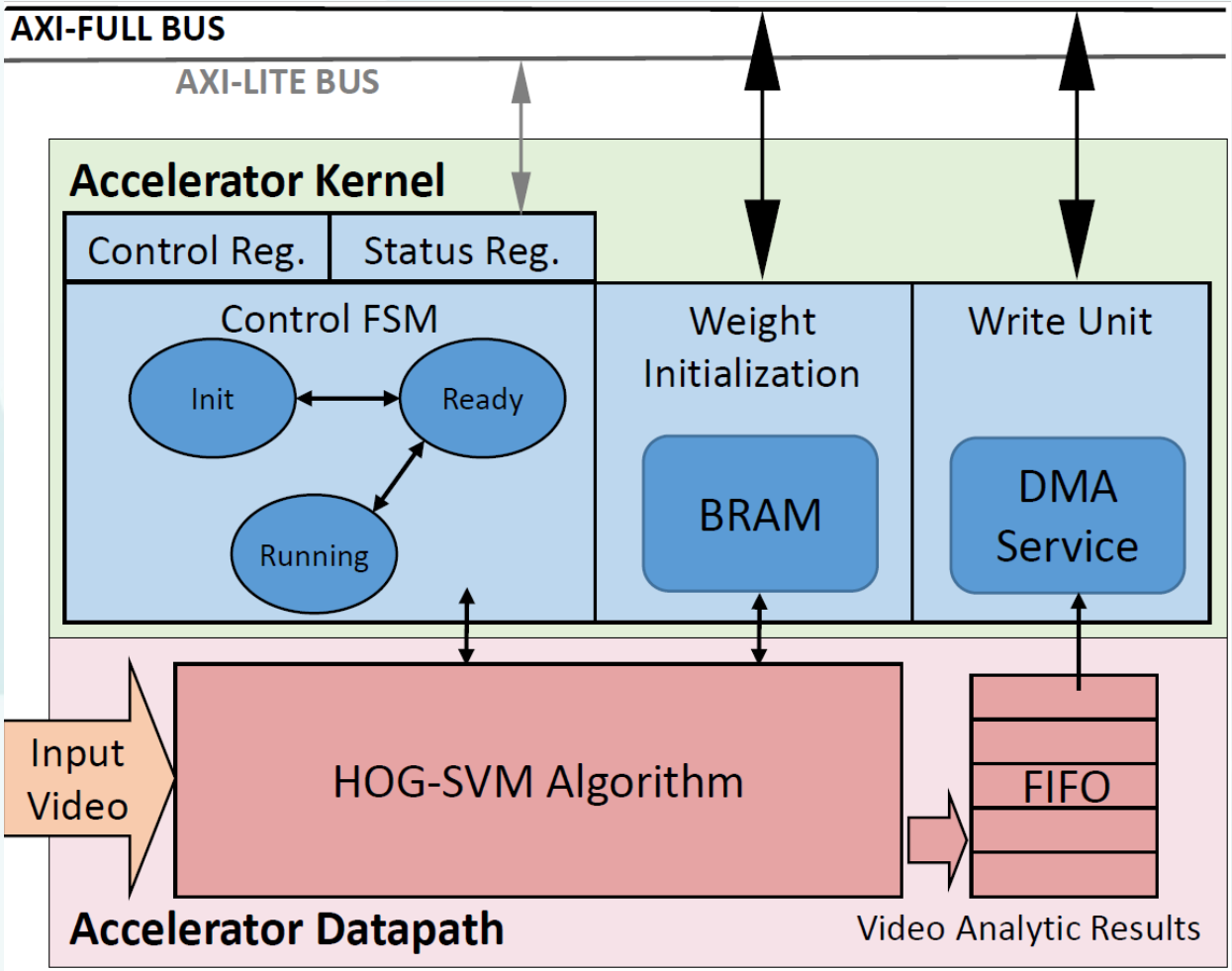
Introduction

- A hardware thread model and bare-metal device drivers were developed which encapsulate the behavior of the accelerator as a hardware thread to the applications running on the ARM CPU.

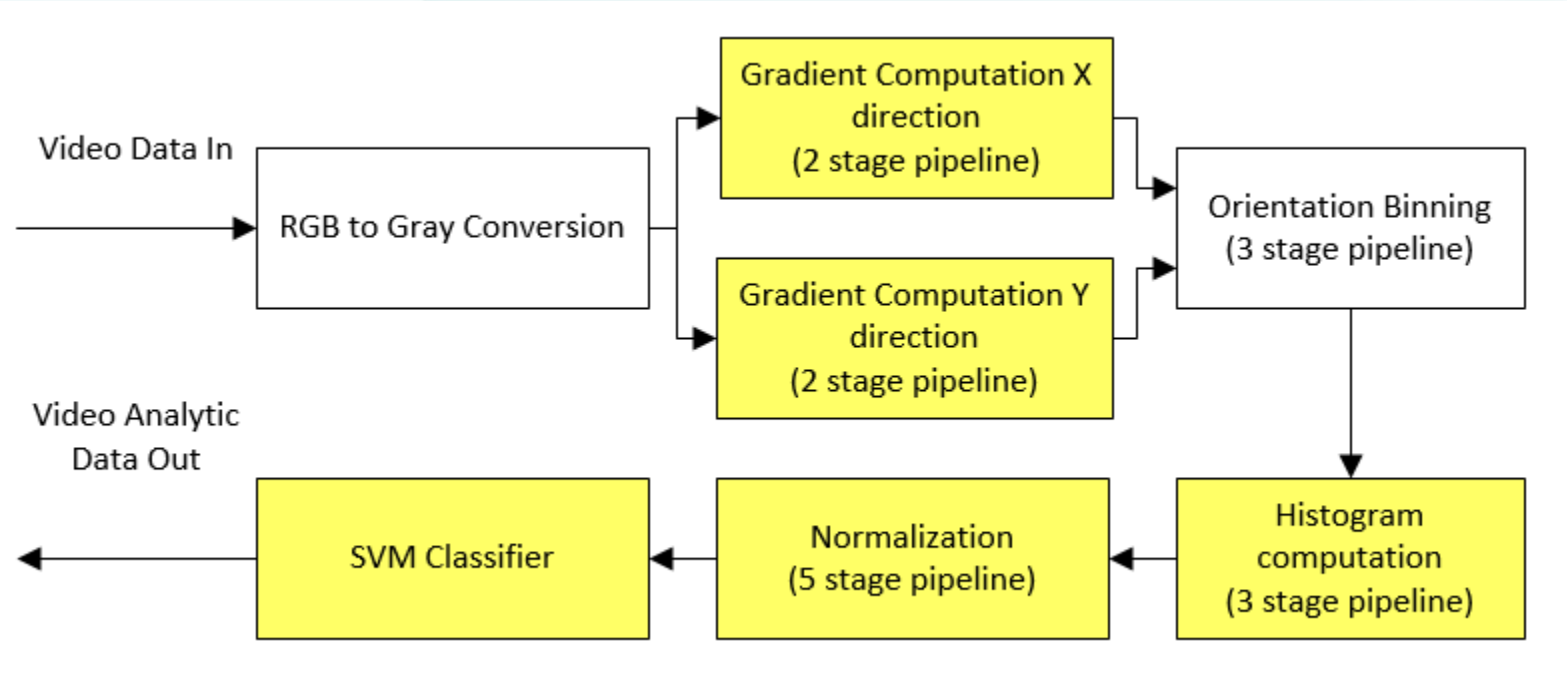
Architecture and Methedology



Architecture and Methedology

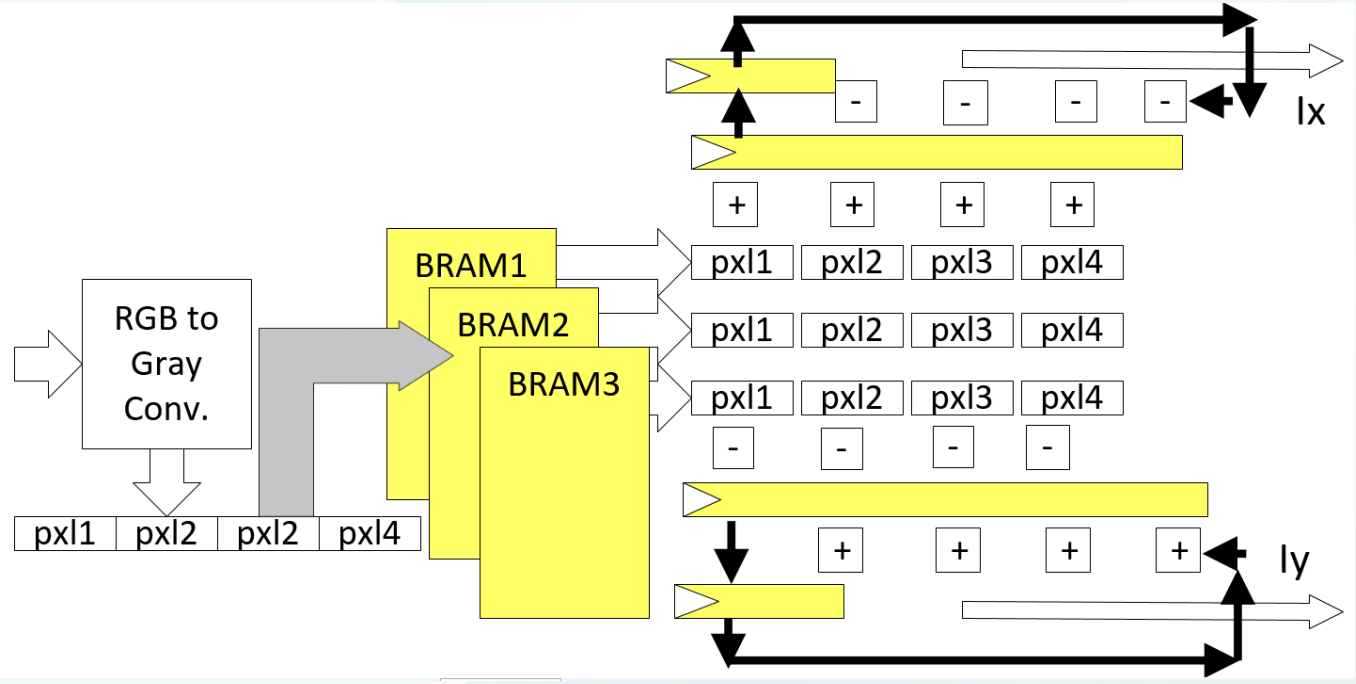


Architecture and Methedology
Deep Pipelined Datapath



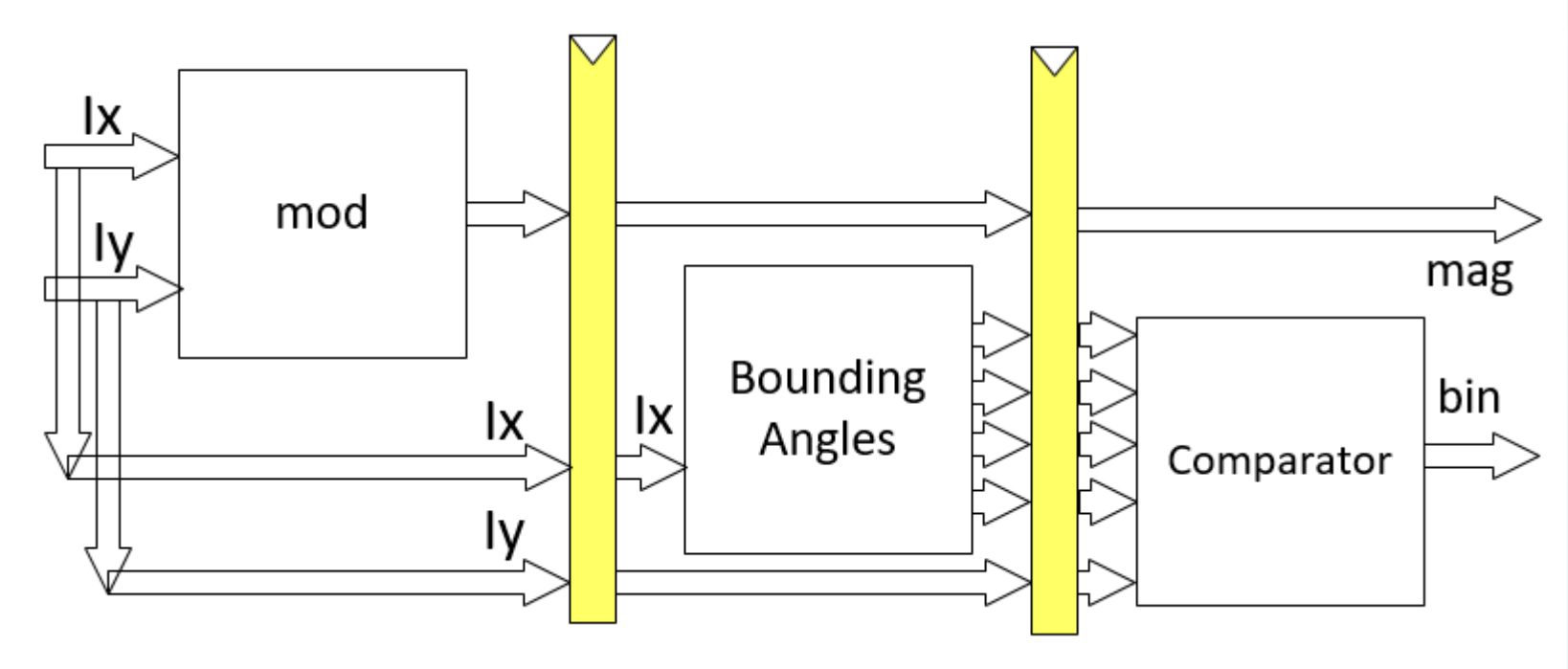
Architecture and Methedology

Front End Pixel Buffer and Gradient Computation Stage



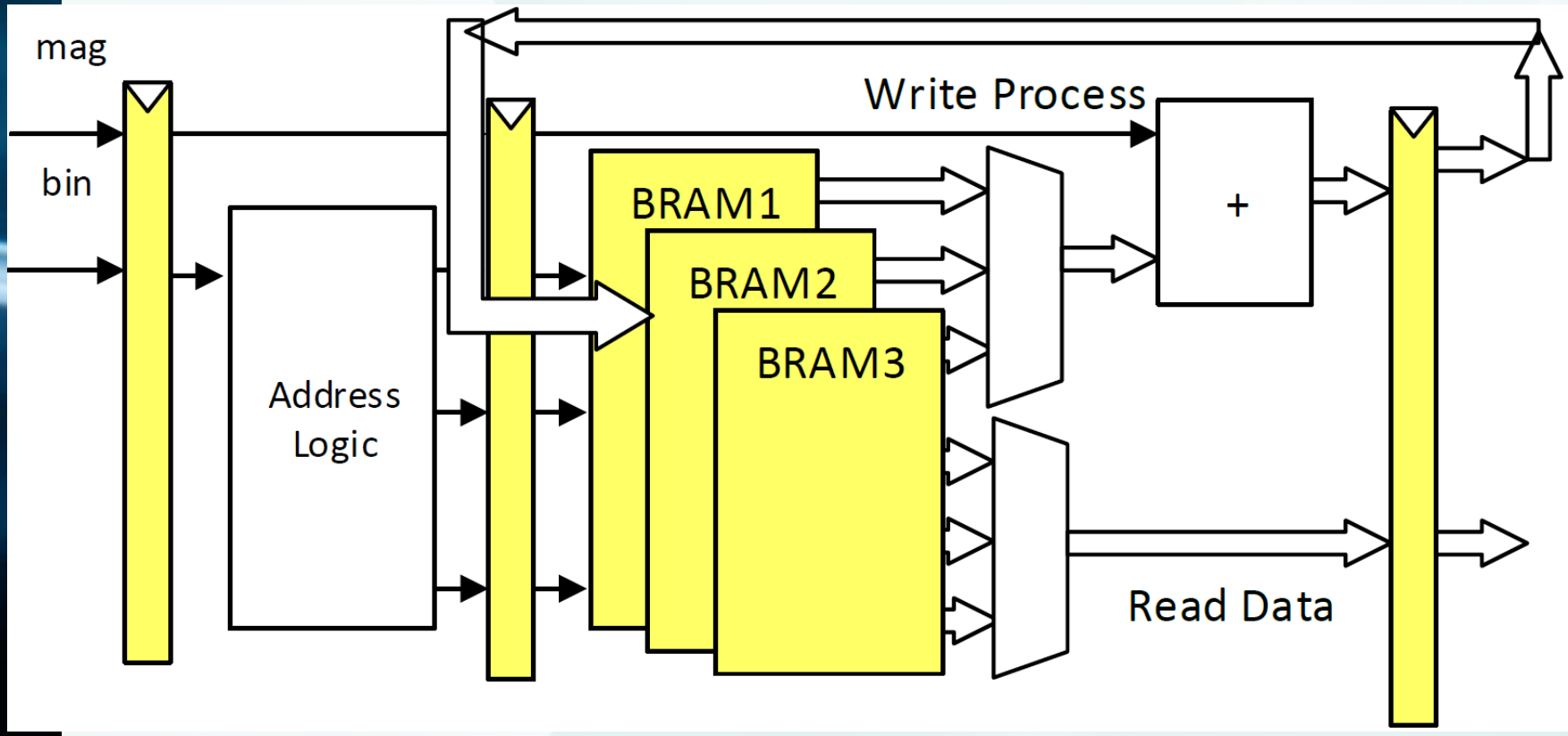
Architecture and Methedology

Orientation Binning Pipeline



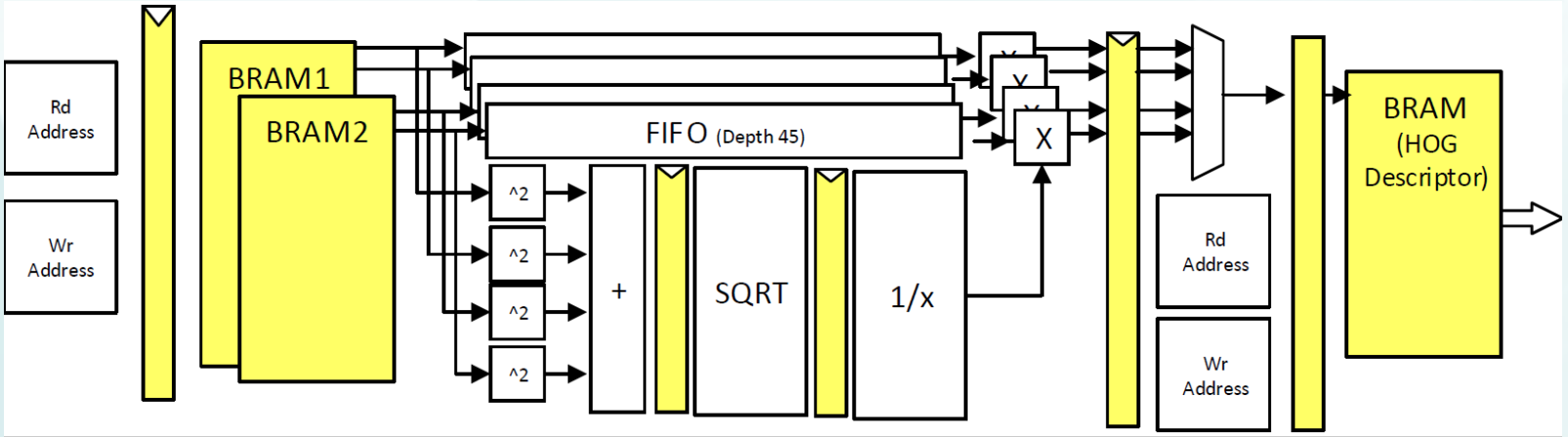
Architecture and Methedology

Histogram Creation Pipeline



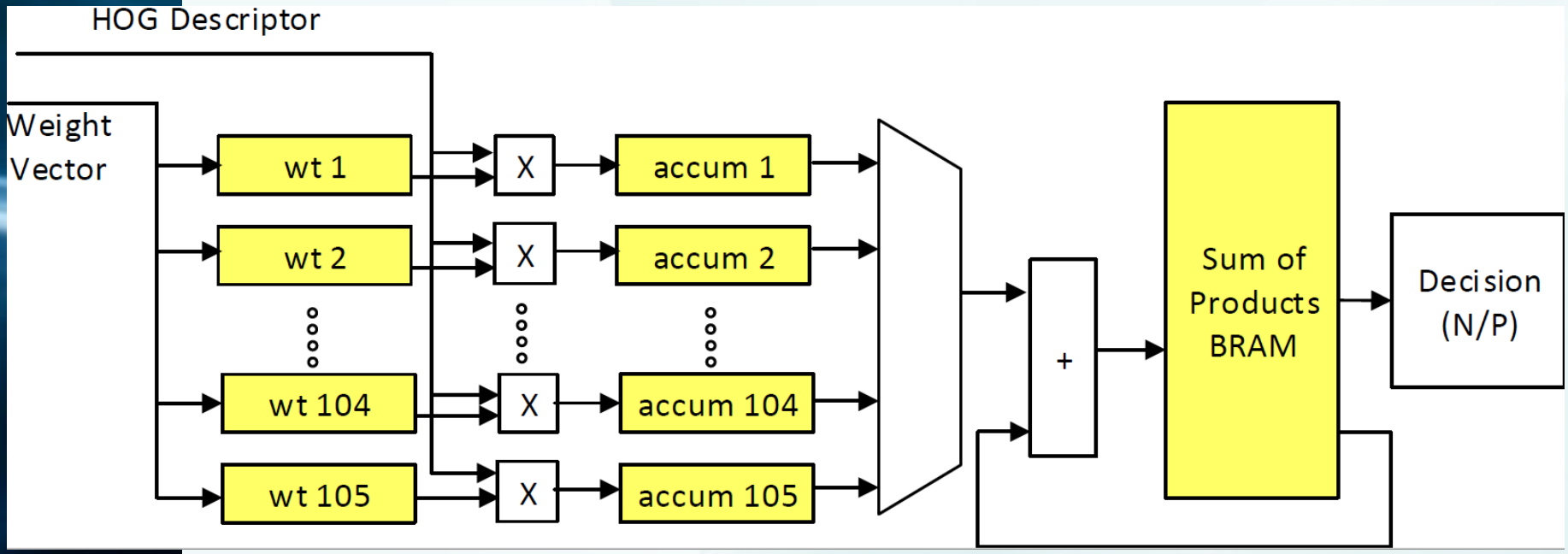
Architecture and Methedology

Normalization Pipeline



Architecture and Methedology

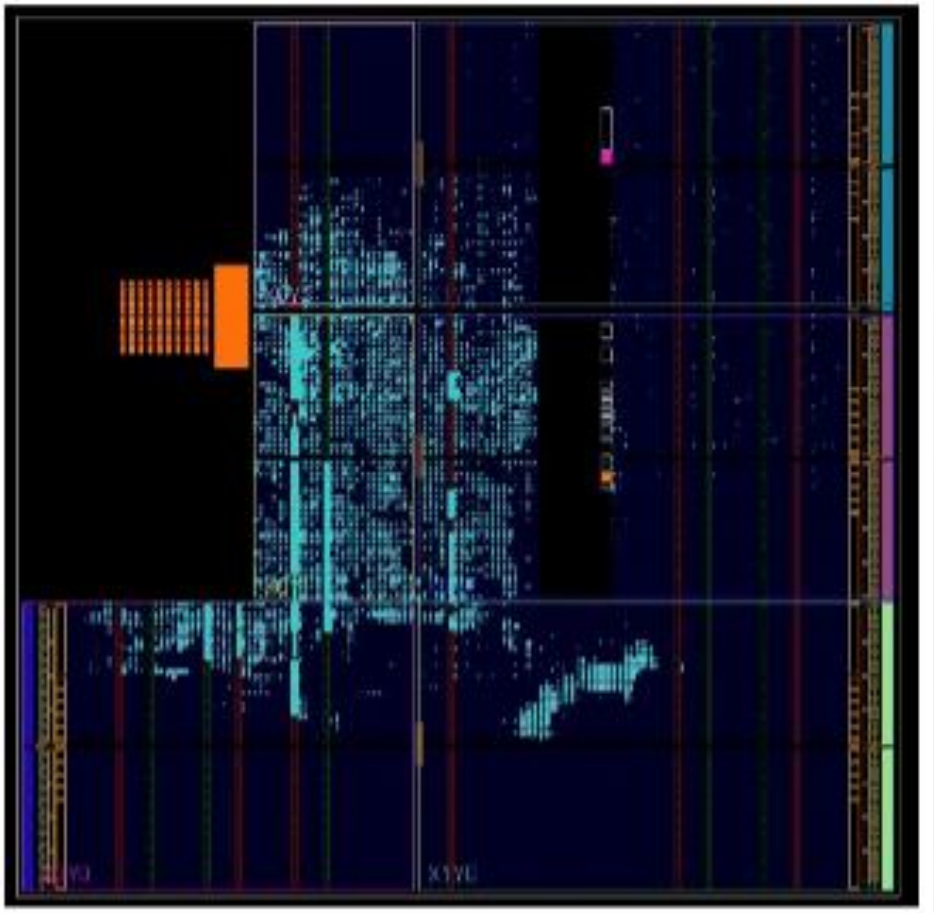
SVM Classifier



Results
Resource Utilization

Module	LUTs	Registers	BRAMs	DSPs
Front Pixel Buffer	36	96	1.5	0
Gradient Computation	232	326	0	0
Hist. Creation	374	242	1.5	7
Normalization	472	359	5	4
SVM Classifier	4615	7287	60.5	106
Write Unit	91	213	4	0
Control Unit	20	11	0	0
AXI Components	82	201	0	0
Video Source	116	88	0	0
Overall design	6069	8841	74.5	117
(XC7Z020)	11.40%	8.30%	53.21%	53.18%

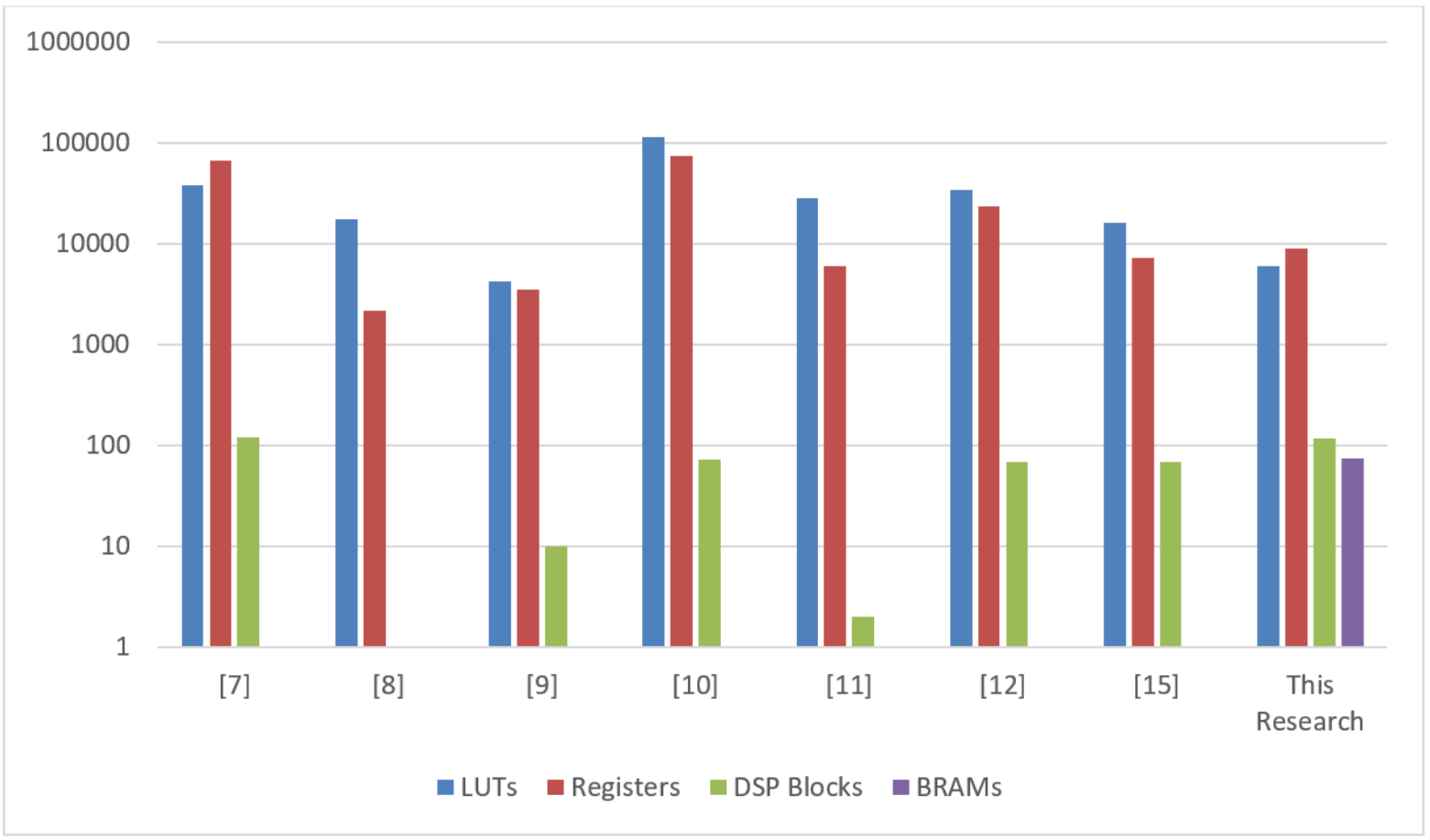
Results
Resource Utilization



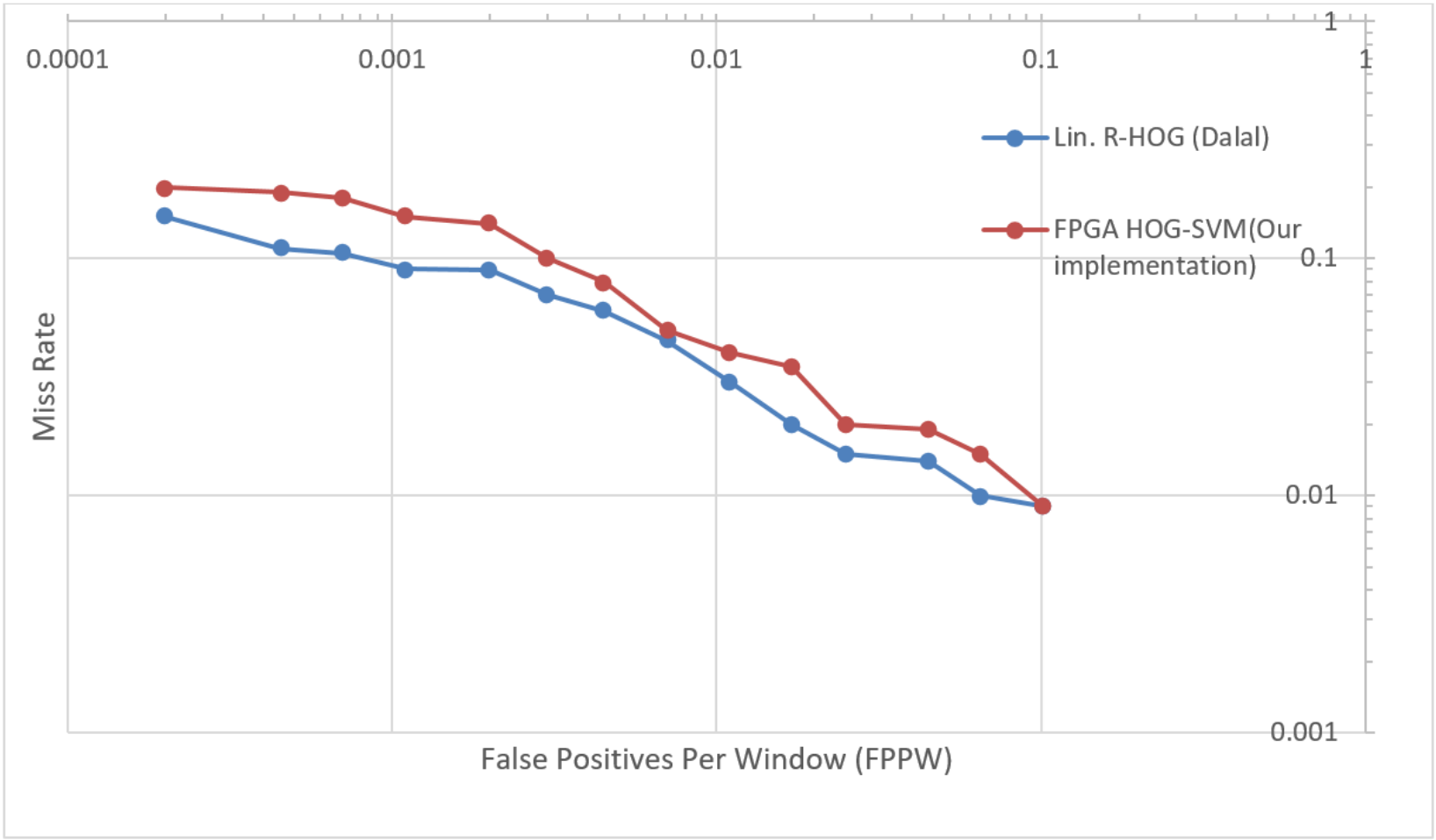
Results
Comparison with Previous Work

	[7]	[8]	[9]	[10]	[11]	[12]	[15]	This Research
Resolution/ Frame Size	640x480	320x240	various	640x480	320x240	800x600	800x600	1920x1080
Frame Rate (fps)	30	62	about 15	60	38	72	162	240
Operating Freequency(MHz)	127	44	192	25	167	40	150	148.5
Platform	Altera Startix II	Xilinx Virtex-5	Xilinx Spartan-6	Xilinx Virtex-6	Xilinx Virtex-5	Altera Cyclone IV	Altera Cyclone IV	Xilinx Zynq 7000
Number of LUTs	37940	17383	4169	113359	28495	34403	16060	6069
Number of Registers	66990	2181	3533	75071	5980	23247	7220	8841
Number of DSP blocks	120	no data	10	72	2	68	69	117
Number of BRAMs	no data	no data	no data	no data	no data	no data	no data	74.5

Results
Resource Utilization Comparison



Results
Comparison of Detection Error



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