F-E3D: FPGA-based Acceleration of an Efficient 3D Convolutional Neural Network for Human Action Recognition

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Motivation

• Human action recognition (HAR)
  – required by demanding applications, e.g. autonomous driving, surveillance…

• Algorithms for HAR with best accuracy
  – 3-dimensional convolutional neural networks (3D CNNs)

• 3D CNN inference on ARM CPU: 0.25 frame per second (fps)
  – does not meet real-time requirements
Challenges

• High Computational Complexity
  – standard 3D-CNNs: at least 3x computations of 2D-CNNs

• Large Numbers of Parameters
  – 3D convolution: parameters in three different dimensions

• Limited Compression Rate
  – By Quantization and 3D Winograd algorithms
Contributions

1. An efficient 3D CNN (E3DNet): better than standard 3D CNNs (C3D)
   - 37 times smaller
   - 5% more accurate on UCF101

2. An FPGA-based architecture (F-E3D)
   - high performance and enhanced hardware efficiency

3. Comprehensive comparison
   - with other 3D CNN models on various platforms
Background: 3D CNNs

- 3D convolution: accumulates results from different frames to generate output feature maps
C3D is one of the most commonly used 3D CNNs for HAR.
Background: Model Compression

- Quantization
  - Linear integer quantization, Binary and Ternary quantization

- Weight Pruning and Approximation
  - Low-Rank Factorization and Structural Matrix

- Efficient Building Blocks
  - Depth-wise convolution and Bottleneck residual block
Background: Depth-wise Convolution

- Without channel accumulation
- Channel number is equal to filter number
Background: Bottleneck Residual Block

- Fewer parameters
- Fewer operations

* BN: Batch Normalization
1. Efficient 3D-CNNs: (a) 3D-1 BRB

- Generalize the BRB to 3D-CNNs
- Expand all 2D convolutions to 3D convolutions
- Temporal kernel size of 3 added to:
  - the first 3D convolution
  - the second 3D convolution
1. Efficient 3D-CNNs: (b) E3DNet

- Similar network structure to MobileNetV2
- 17 3D-1 BRBs
- Input size: 16 x 112 x 112 x 3

<table>
<thead>
<tr>
<th>Input</th>
<th>Operation</th>
<th>$t$</th>
<th>$N_f$</th>
<th>$n$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$16 \times 112^2 \times 3$</td>
<td>Conv $1 \times 3 \times 3$</td>
<td>-</td>
<td>45</td>
<td>1</td>
</tr>
<tr>
<td>$16 \times 56^2 \times 45$</td>
<td>Conv $3 \times 1 \times 1$</td>
<td>-</td>
<td>64</td>
<td>1</td>
</tr>
<tr>
<td>$16 \times 56^2 \times 64$</td>
<td>3D-1 BRB</td>
<td>1</td>
<td>24</td>
<td>1</td>
</tr>
<tr>
<td>$16 \times 56^2 \times 24$</td>
<td>3D-1 BRB</td>
<td>6</td>
<td>24</td>
<td>2</td>
</tr>
<tr>
<td>$16 \times 56^2 \times 24$</td>
<td>3D-1 BRB</td>
<td>6</td>
<td>48</td>
<td>4</td>
</tr>
<tr>
<td>$8 \times 28^2 \times 48$</td>
<td>3D-1 BRB</td>
<td>6</td>
<td>64</td>
<td>6</td>
</tr>
<tr>
<td>$4 \times 14^2 \times 64$</td>
<td>3D-1 BRB</td>
<td>6</td>
<td>96</td>
<td>3</td>
</tr>
<tr>
<td>$2 \times 7^2 \times 96$</td>
<td>3D-1 BRB</td>
<td>6</td>
<td>512</td>
<td>1</td>
</tr>
<tr>
<td>$2 \times 7^2 \times 512$</td>
<td>GAP</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$1 \times 1^2 \times 512$</td>
<td>Conv $1 \times 1 \times 1$</td>
<td>-</td>
<td>$k$</td>
<td>1</td>
</tr>
</tbody>
</table>
2. Design Methodology: (a) Fused 3D BRB

- Memory-bound if accelerate each layer separately
- Cache the intermedia results within 3D-1 BRB on chip
2. Design Methodology: (b) Online Blocking

- Large on-chip memory requirement
- Online Blocking: Controlling the computational flow
2. Design Methodology: (c) Kernel Reuse

- Map 1x1x1 and 3x1x1 convolution into the computational kernel of 3D depth-wise convolution

Algorithm 2 Kernel Reuse with Temporal Convolution.

1: for \( frm = 0 \) to \( N_l \) do
2:   for \( f_{th} = frm \) to \( frm + K_t \) do  \( \triangleright \) Loop Interchange
3:     for \( fltr = 0 \) to \( N_f \) do
4:       for \( c = 0 \) to \( N_c \) do  \( \triangleright \) Loop Unrolling
5:         for \( c = 0 \) to \( \frac{N_c}{K_{dw} \times K_{dw}} \) do
6:           for \( h = 0 \) to \( H \) do
7:             for \( w = 0 \) to \( W \) do
8:               for \( c_{unrol} = c \times K_{dw}^2 \) to \( (c + 1) \times K_{dw}^2 \) do
9:                 for \( f_{th} = frm \) to \( frm + K_t \) do
10:                  \( \text{outpt}[frm][fltr][h][w] += \)
11:                  \( \text{coef}[f_{th}][fltr][c_{unrol}] \times \)
12:                  \( \text{inpt}[f_{th}][c_{unrol}][h][w]; \)
3. Hardware Design: (a) Architecture

- mainly consists of a computational engine, sliding window, ReLU, pooling modules and several buffers.
4. Experiment: (a) Setting

- Intel Arria 10SX 660 platform: using Verilog toolchain

- Human action recognition on UCF101: 13320 videos of 101 human action categories

- Input shape:
  16 X 112 X 112 X 3
4. Experiment: (b) Model Size and Accuracy

- 37 times smaller and 5% more accurate than C3D

<table>
<thead>
<tr>
<th></th>
<th>E3DNet</th>
<th>ResNeXt-101</th>
<th>P3D</th>
<th>C3D</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clip@1 Accuracy</td>
<td>85.17%</td>
<td>87.7%</td>
<td>84.2%</td>
<td>79.87%</td>
</tr>
<tr>
<td>Model Size</td>
<td>8.6MB</td>
<td>365MB</td>
<td>261MB</td>
<td>321MB</td>
</tr>
<tr>
<td>Compression Rate</td>
<td>Baseline</td>
<td>42.3</td>
<td>30.3</td>
<td>37.3</td>
</tr>
<tr>
<td>MAdds</td>
<td>6.1G</td>
<td>9.8G</td>
<td>19.2G</td>
<td>38.2G</td>
</tr>
<tr>
<td>Operation Reduction</td>
<td>Baseline</td>
<td>1.6</td>
<td>3.1</td>
<td>6.2</td>
</tr>
</tbody>
</table>
4. Experiment: (c) FPGA Design

- Avalon memory mapped interface (Avalon-MM)
4. Experiment: (c) FPGA Design

- Resource consumption of FPGA design

<table>
<thead>
<tr>
<th></th>
<th>ALMs</th>
<th>DSPs</th>
<th>M20K</th>
</tr>
</thead>
<tbody>
<tr>
<td>Available</td>
<td>251680</td>
<td>1687</td>
<td>2133</td>
</tr>
<tr>
<td>Utilization</td>
<td>113828</td>
<td>1584</td>
<td>1578</td>
</tr>
<tr>
<td>Percentage Used</td>
<td>45.2%</td>
<td>93.3%</td>
<td>74%</td>
</tr>
</tbody>
</table>
4. Experiment: (d) FPGA Performance Comparison

- Nearly the same performance with GPU with less energy
- 13 times faster previous FPGA design

<table>
<thead>
<tr>
<th></th>
<th>CPU</th>
<th>GPU</th>
<th>FPGA</th>
<th>Our Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Platform</td>
<td>Intel Xeon E5-2680 v2</td>
<td>TITAN X Pascal</td>
<td>Xilinx ZC706</td>
<td>Intel Arria 10 SX660</td>
</tr>
<tr>
<td>Frequency</td>
<td>2.8 GHz</td>
<td>1.53 GHz</td>
<td>200 MHz</td>
<td>150 MHz</td>
</tr>
<tr>
<td>Model</td>
<td>E3DNet</td>
<td>E3DNet</td>
<td>C3D+SVM</td>
<td>E3DNet</td>
</tr>
<tr>
<td>Precision</td>
<td>32bit-float</td>
<td>32bit-float</td>
<td>block-float</td>
<td>32bit-float</td>
</tr>
<tr>
<td>Accuracy</td>
<td>85.17%</td>
<td>85.17%</td>
<td>&lt; 81.99%</td>
<td>85.17%</td>
</tr>
<tr>
<td>Power (W)</td>
<td>135</td>
<td>240</td>
<td>9.9</td>
<td>36</td>
</tr>
<tr>
<td>Latency (ms)</td>
<td>6921.3</td>
<td>41.1</td>
<td>476.8</td>
<td>35.3</td>
</tr>
</tbody>
</table>
4. Experiment: (e) Comparison with Other 3D-CNNs

- The second place in accuracy and speed with the least power consumption

![Graph comparing accuracy, latency, and power consumption for different 3D-CNNs](image)

- Dot size is proportional to power consumption.
Future Work

• Further Improve E3DNet accuracy
  – for human action recognition

• Explore 3D-1 BRB
  – for other 3D computer vision tasks such as medical image diagnosis

• Optimize performance of 3D-1 BRB
  – for other technologies, e.g. CPU, GPU, ASIC
Summary

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   – with other 3D CNN models on various platforms

Code available at: https://github.com/os-hxfan/E3DNet.git