A Programmable Architecture for Robot Motion Planning Acceleration

Sean Murray, Will Floyd-Jones,
George Konidaris, Daniel J. Sorin

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DUKE COMPUTER SCIENCE

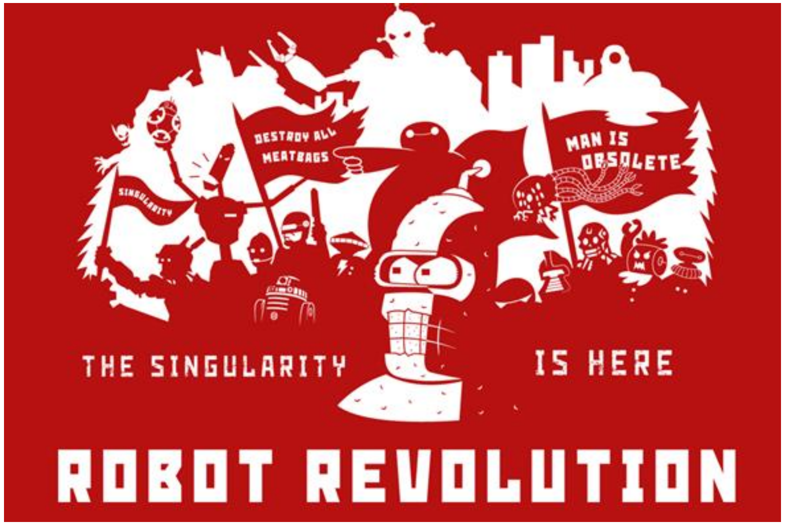
Duke ELECTRICAL & COMPUTER ENGINEERING

Outline

- Background/Previous Work
- Reconfigurable Collision Detection Accelerator
- Hardware-Accelerated Shortest Path
- Conclusions

The State of Robotics

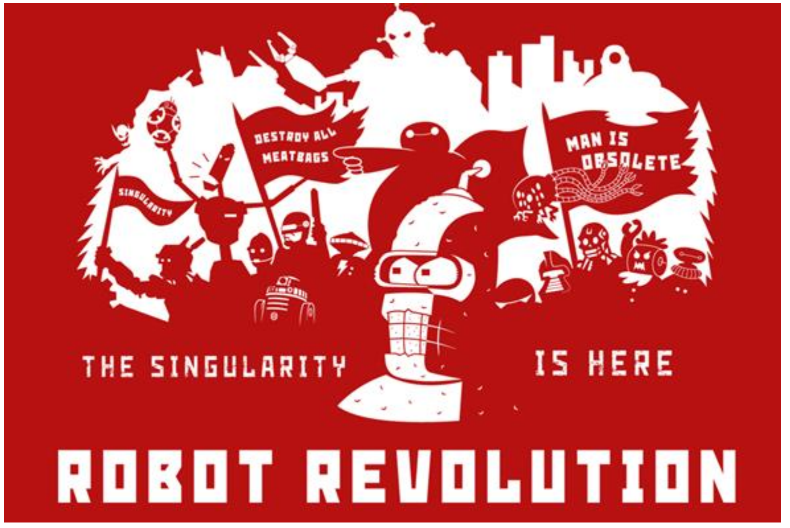
- Modern robots easily capable of submillimeter precision and repeatability
- Becoming a commodity
- Last 10 years the cost of 3D sensors has come down dramatically



- So…Where are all the robots?

The State of Robotics

- Modern robots easily capable of submillimeter precision and repeatability

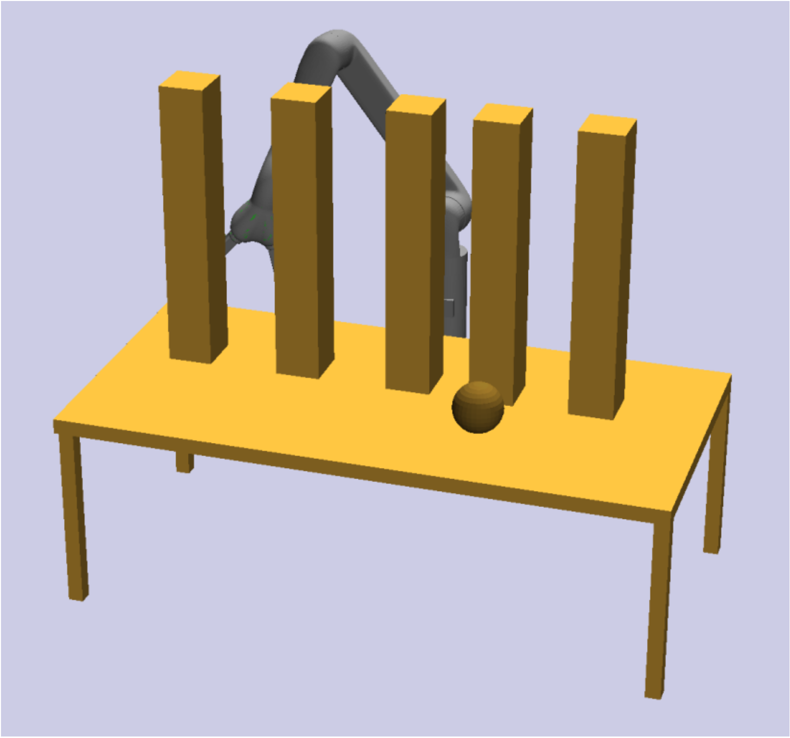


- Becoming a commodity
- Last 10 years the cost of 3D sensors has come down dramatically
- So…Where are all the robots?

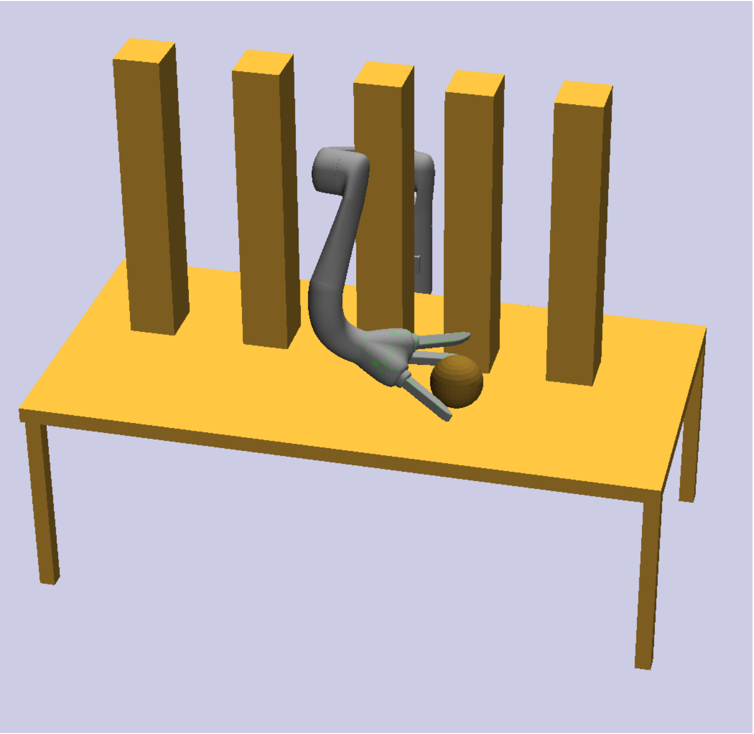
Current motion planning solutions not good enough to allow massive growth into new domains

Problem Description

Motion Planning is the process of finding a collision-free path from a starting configuration to a goal configuration of the robot

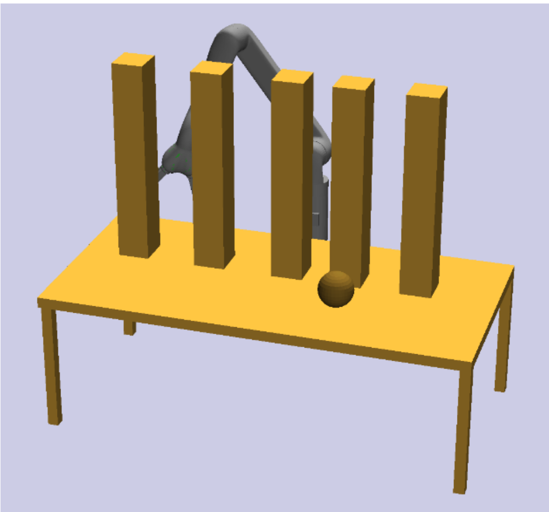


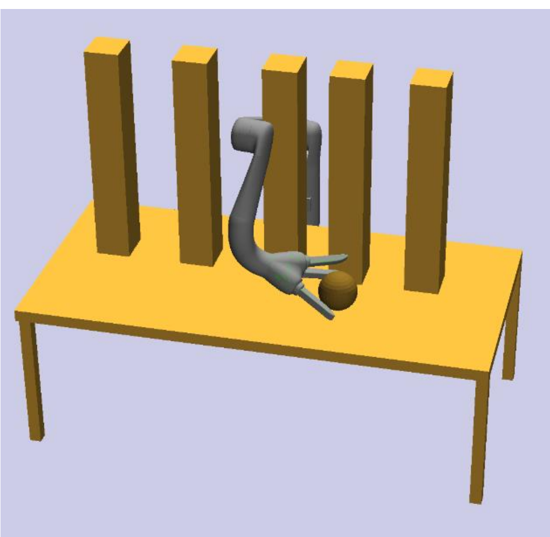
Starting Pose



Goal Pose

Problem Description





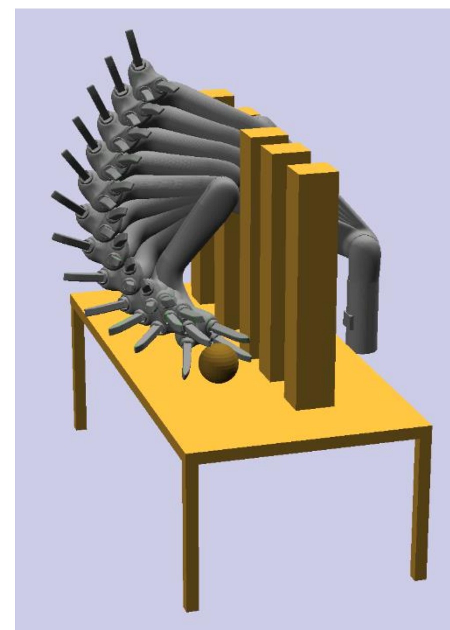
Input

$<C_s, C_g, O>$

C_s = Starting Configuration

C_g = Goal Configuration(s)

O = Description of Obstacles



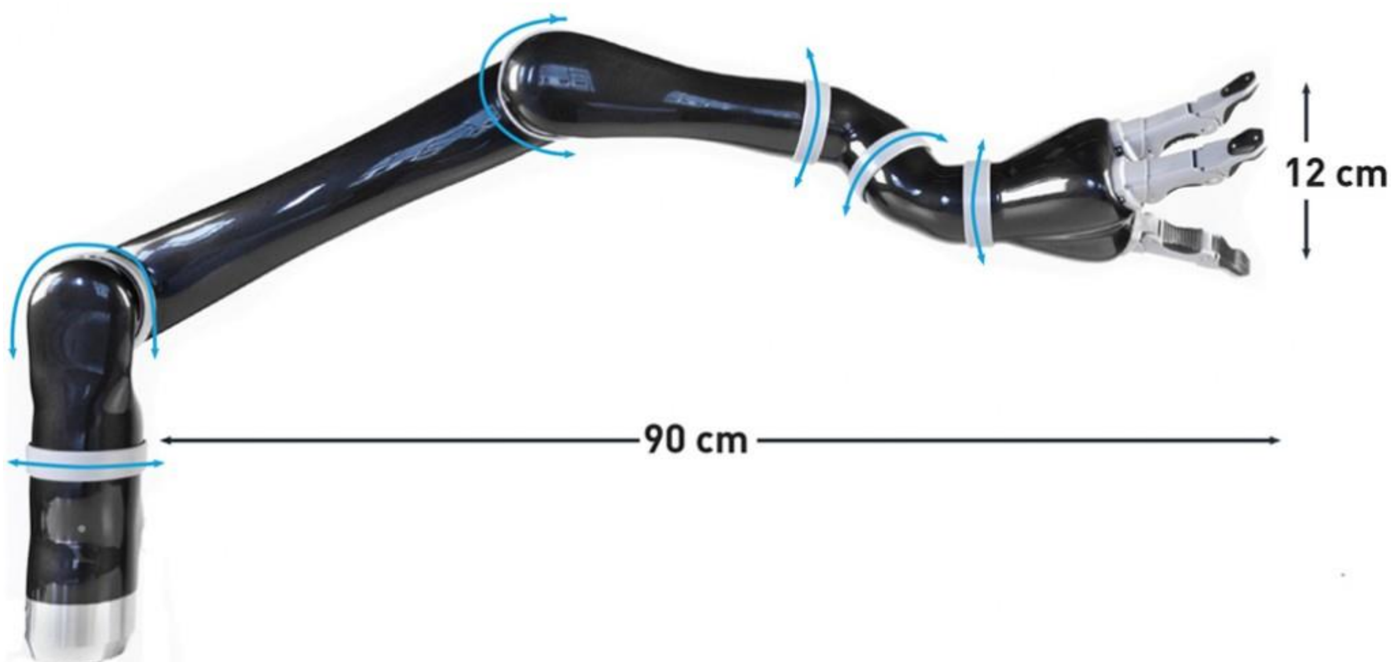
Output

$<P>$

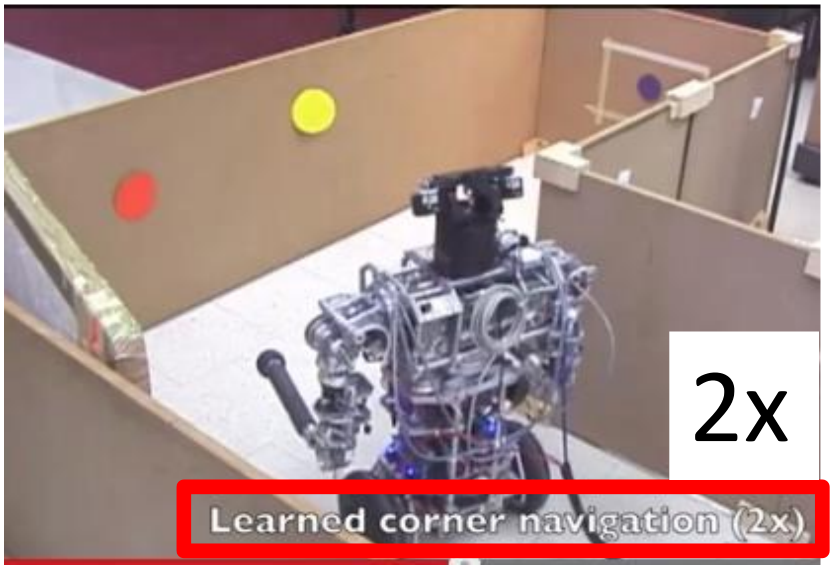
P = a vector of configuration milestones which represents a path

Challenges

- Motion planning suffers from familiar state space explosion problem



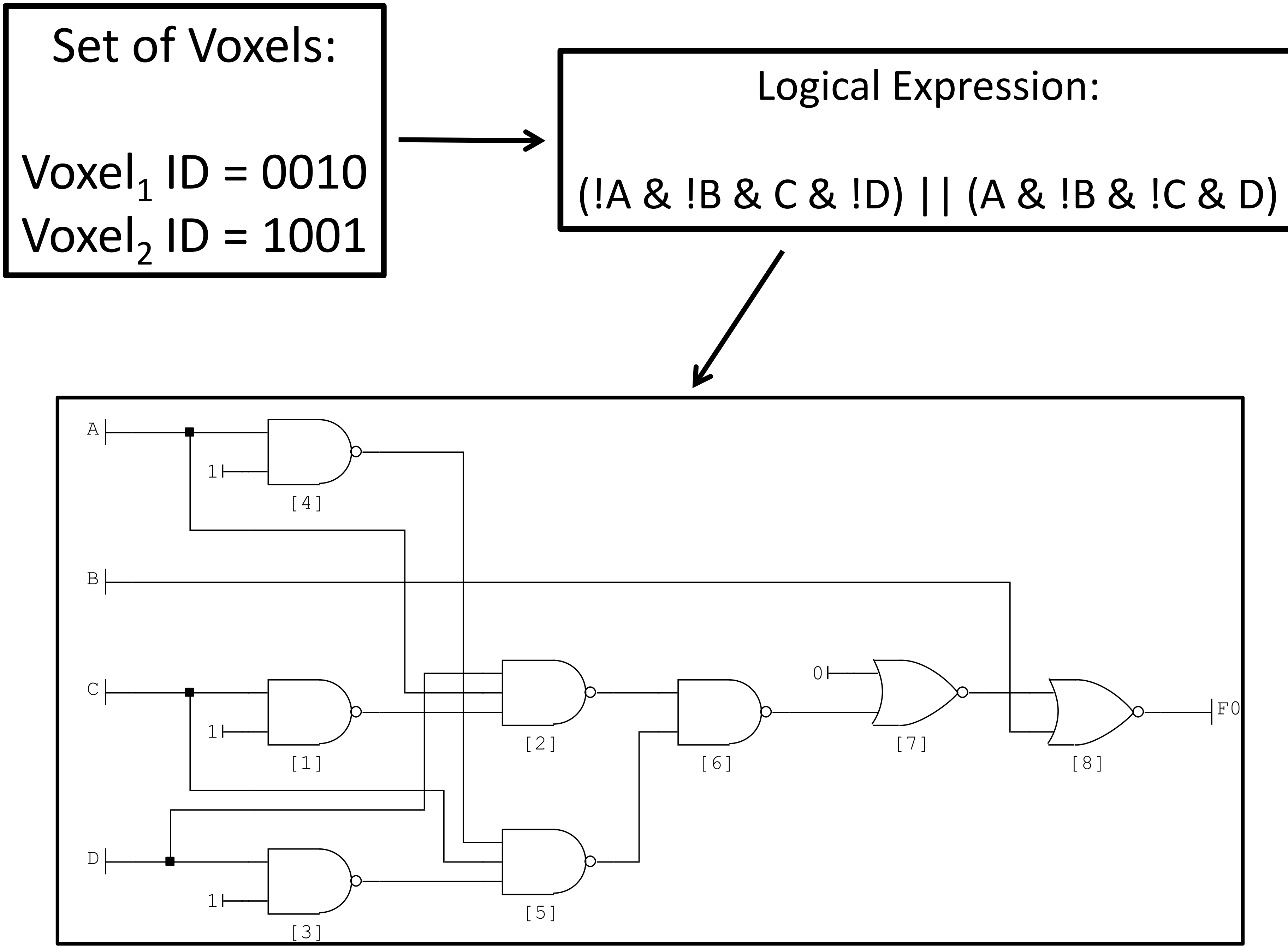
Motion Planning Is Slow



Problem Statement

- The speed of motion planning is a major hindrance to the expansion of robotics
- Our work tries to answer the following research question:

Can we, through a combination of hardware acceleration and algorithm development, alleviate or remove motion planning latency as a pain point?


Set of Voxels:
Voxel$_1$ ID = 0010
Voxel$_2$ ID = 1001
Logical Expression:
(!A & !B & C & !D) || (A & !B & !C & D)
A
B
C
D
1
1
1
0
[4]
[1]
[2]
[3]
[5]
[6]
[7]
[8]
F0

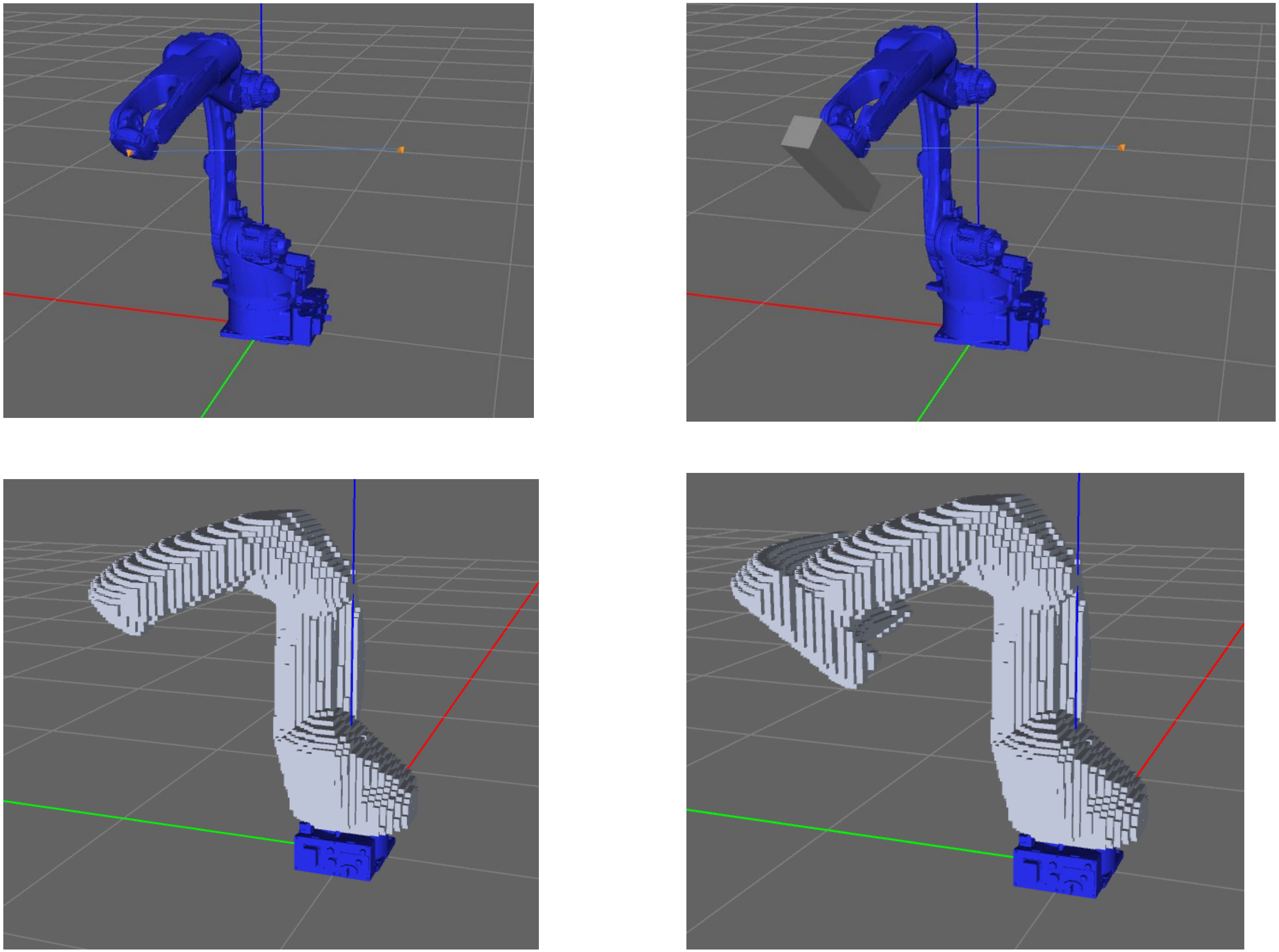
The Need for Configurability

- Previous design was limited to around 3000-motion roadmaps (on one of the largest FPGAs available)

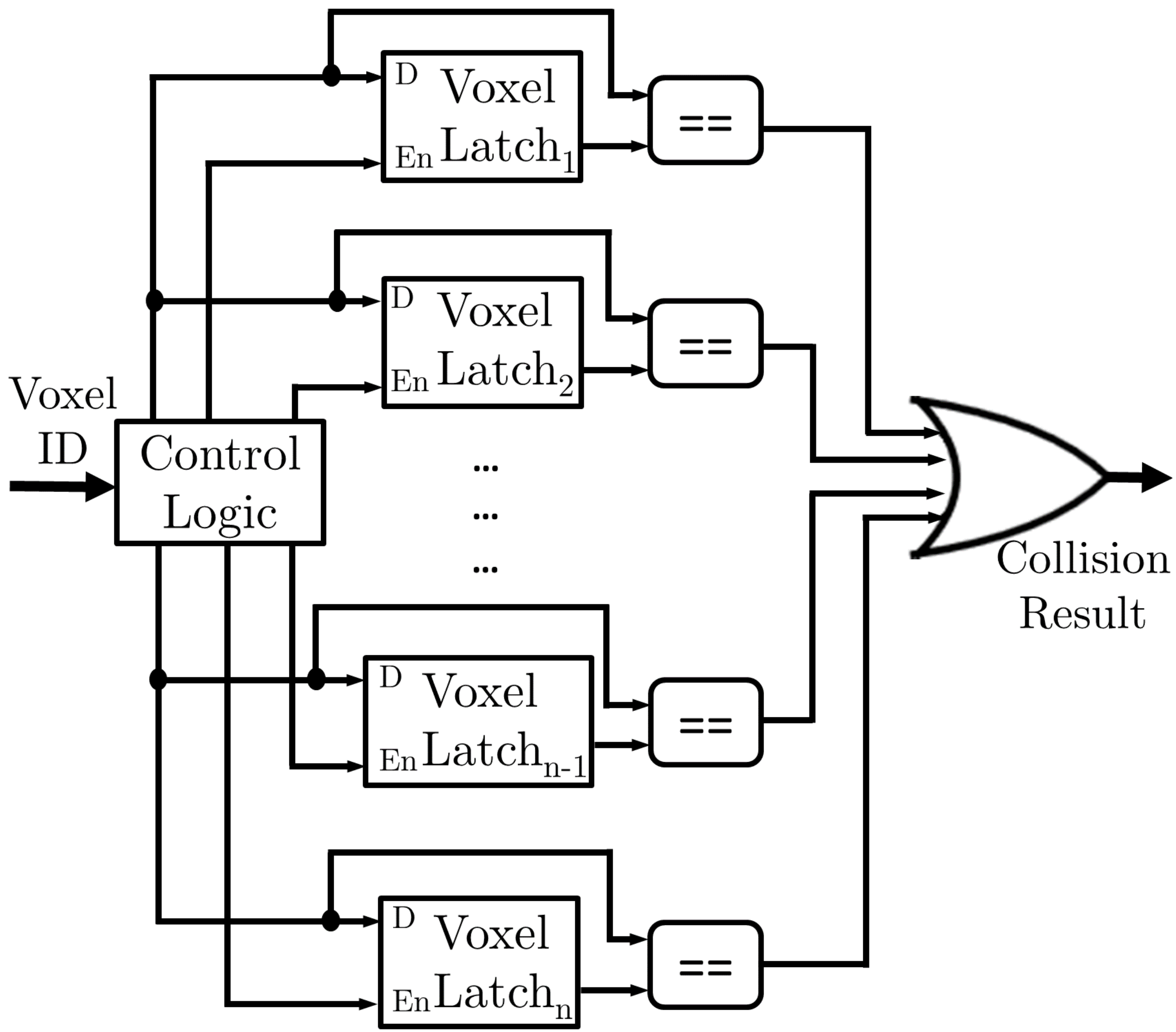
- To handle larger roadmaps, would need to move away from FGPA platform.

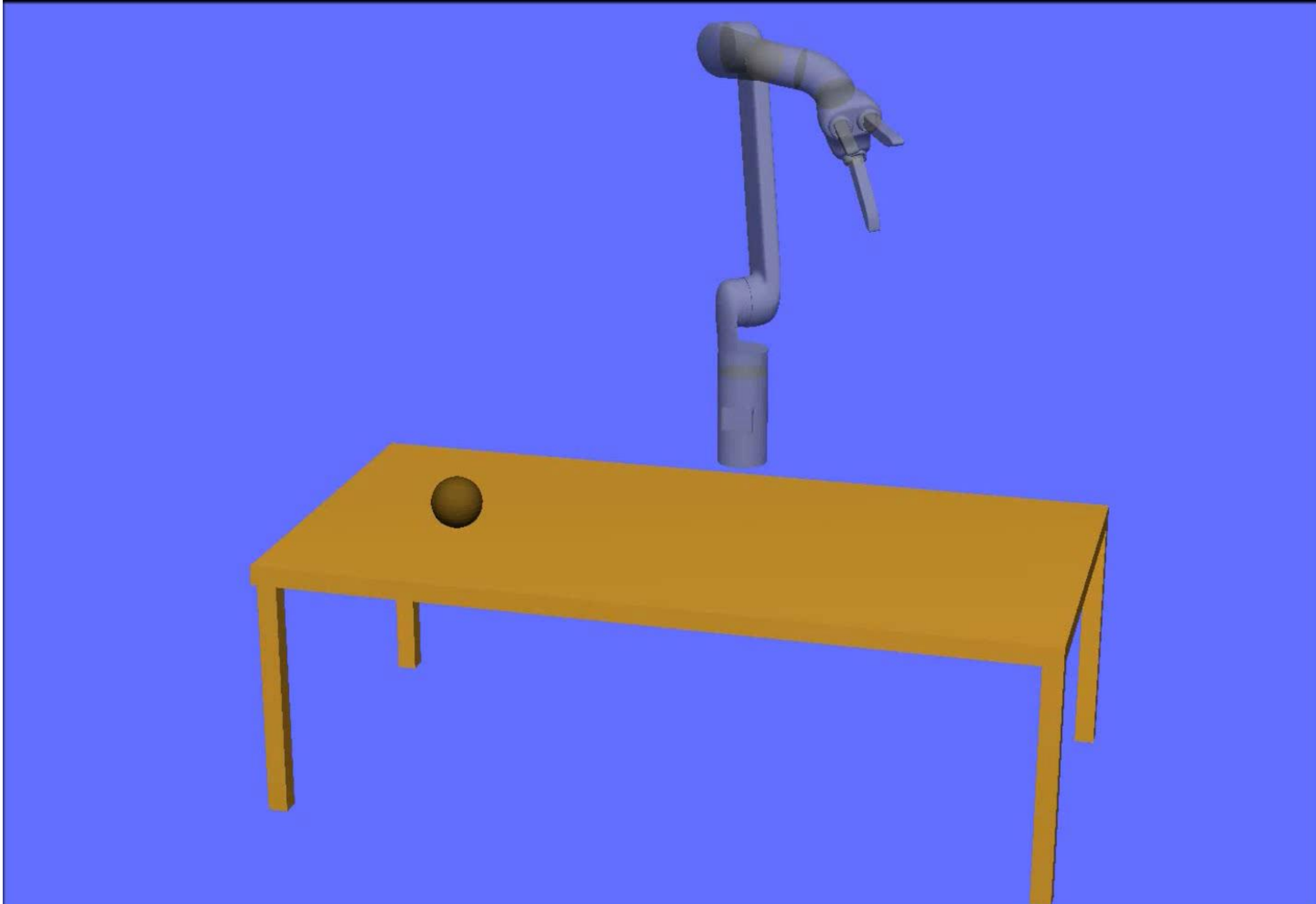
- Can’t justify ASIC cost without flexibility to apply to many robots

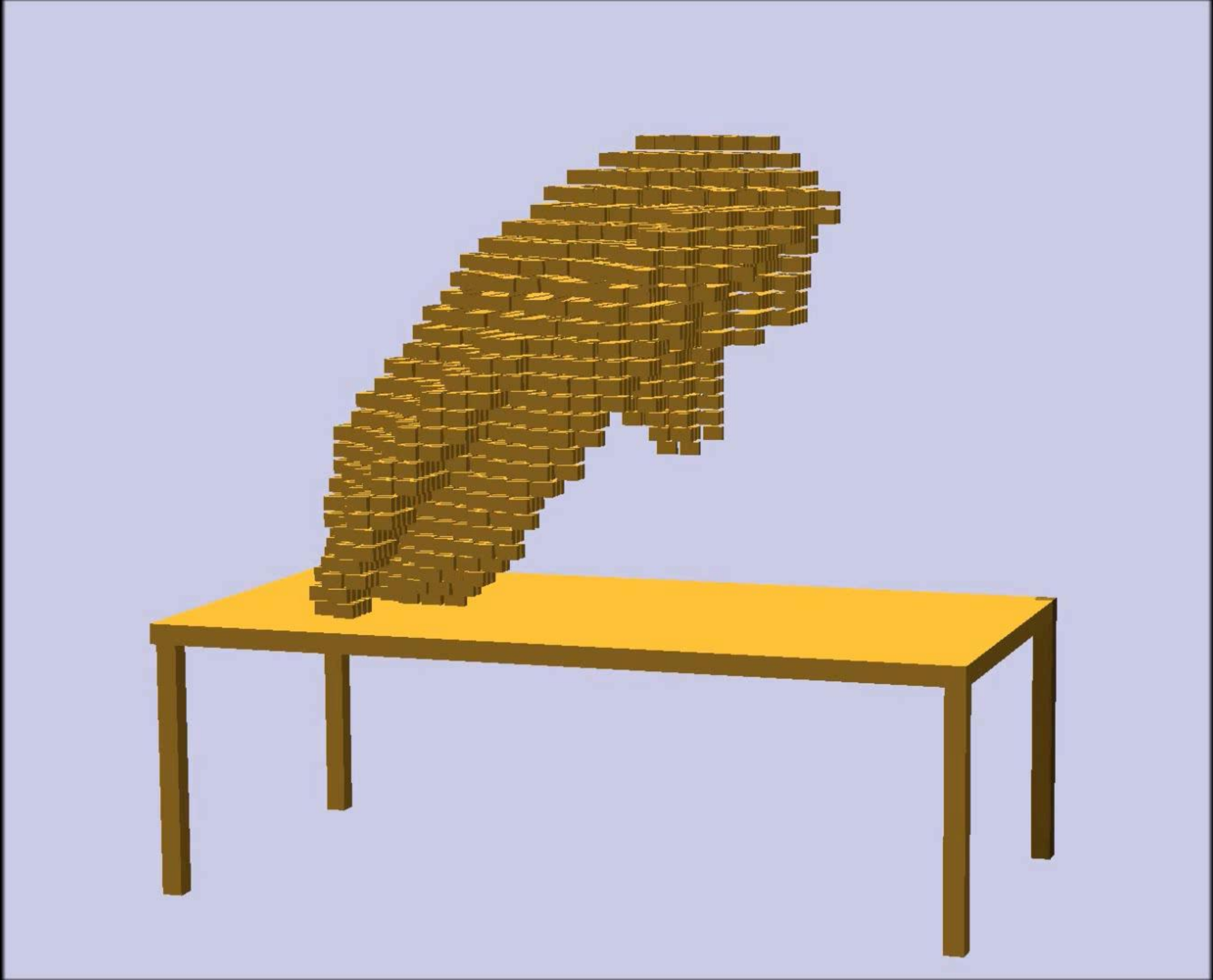
- Even for single robot, its configuration space may change frequently



Reconfigurable Collision Detection



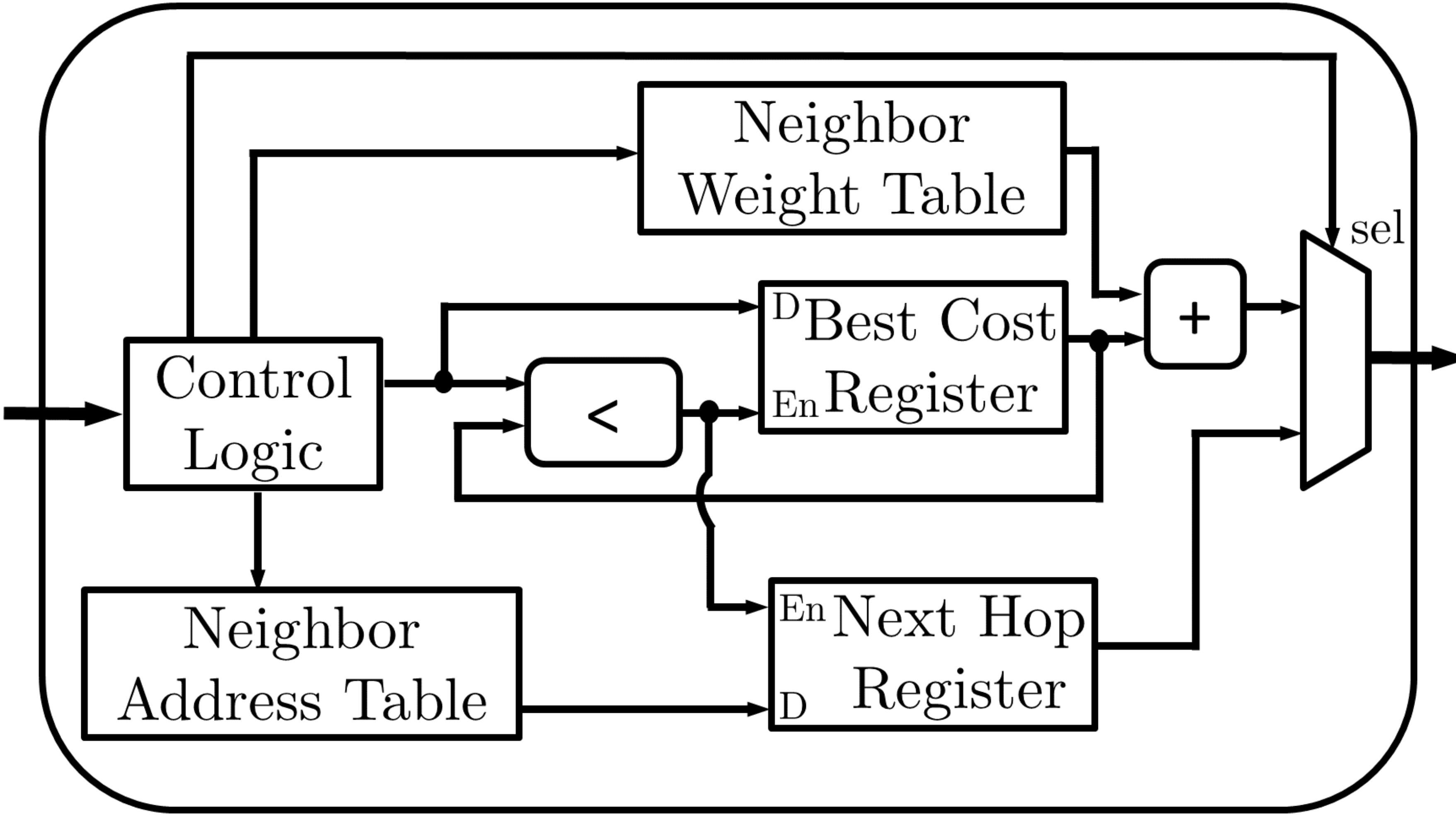


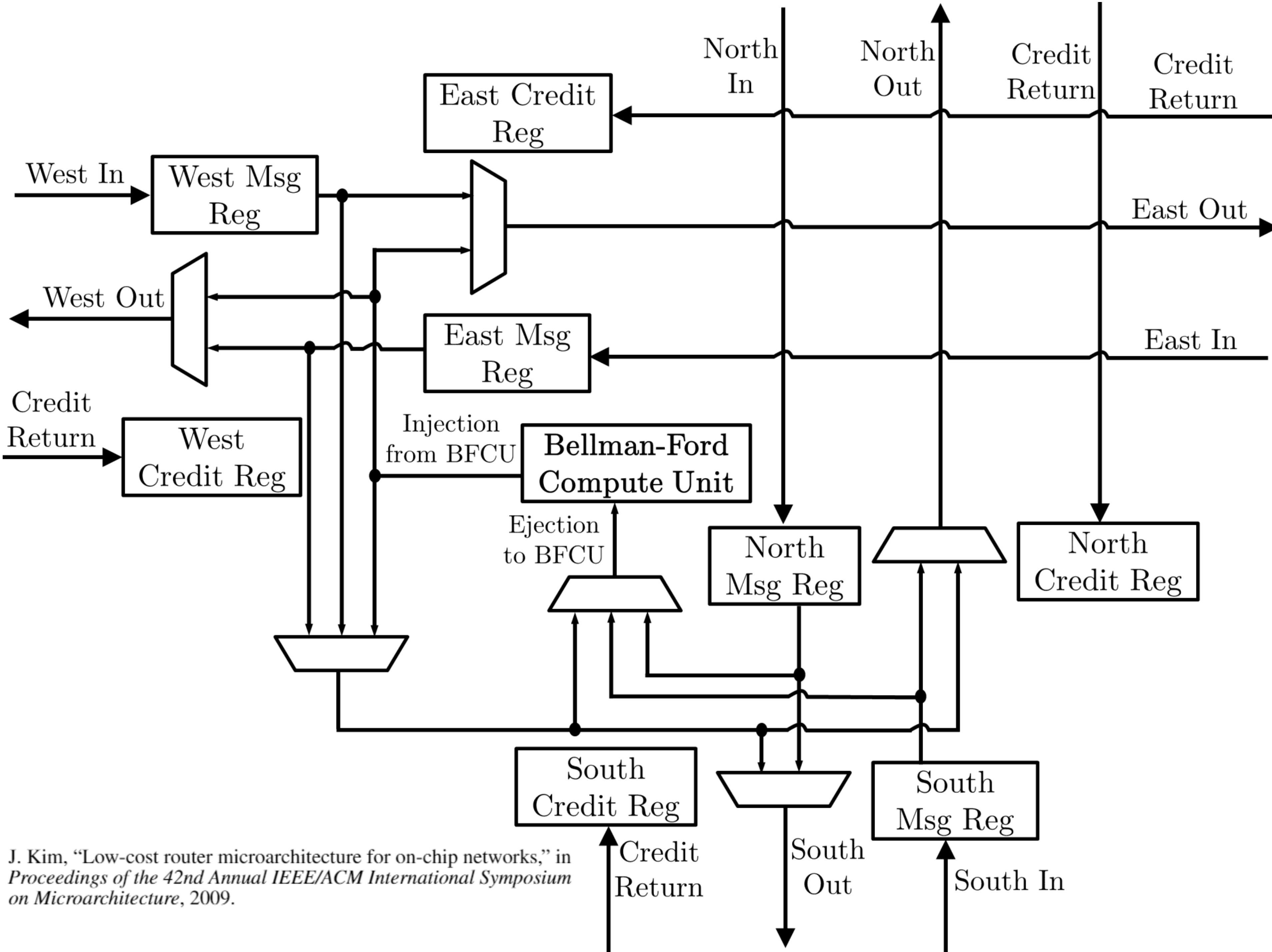


Shortest Path Acceleration

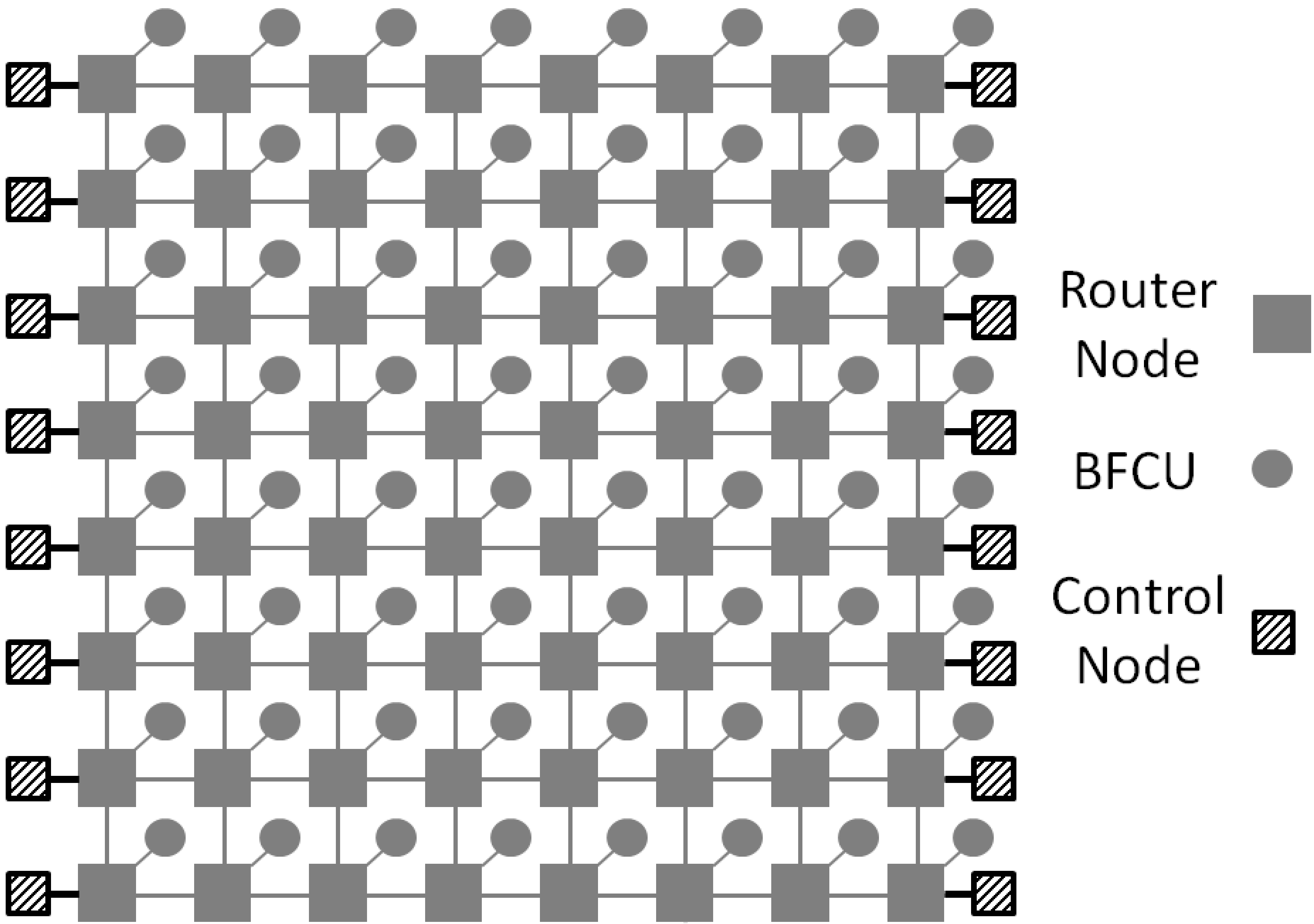
- Shortest Path is the bottleneck if accelerating collision detection
- Would like to bring its latency in line with collision detection for pipelining purposes

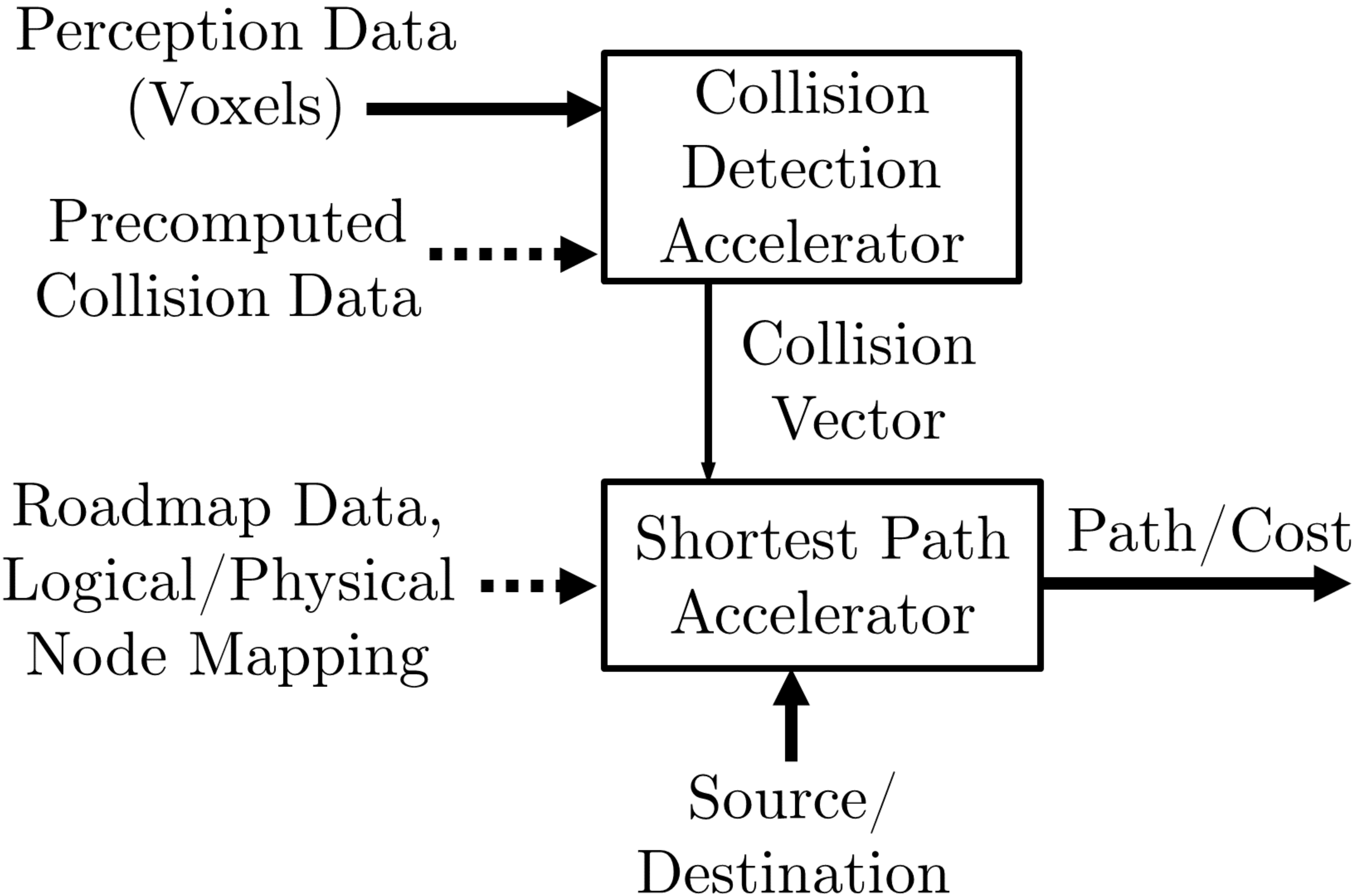
Programmable Bellman-Ford Compute Units





J. Kim, "Low-cost router microarchitecture for on-chip networks," in *Proceedings of the 42nd Annual IEEE/ACM International Symposium on Microarchitecture*, 2009.


Router Node
BFCU
Control Node


Perception Data
(Voxels)
Precomputed
Collision Data
Collision
Detection
Accelerator
Collision
Vector
Roadmap Data,
Logical/Physical
Node Mapping
Shortest Path
Accelerator
Path/Cost
Source/
Destination

Results

- Used Synopsys Nangate 15 nm Open Cell Library to obtain power/area/timing estimates

- For 128 x 128 node design
  - Can be clocked at 1 GHz.
  - 35 Watts Power consumption
  - ~450mm^2 area footprint

Latency Components

- Collision detection: 750 cycles
- Path Search: 630 cycles
- Data transfer: 950 cycles

- Total: less than 2.5 microseconds @ 1 GHz.

Conclusions

- Both collision detection and shortest path at the microsecond level of latency
- Design reconfigurable, makes it more suitable for ASIC-hardening
- Opens up new opportunities such as
  - Planning in environments that change rapidly
  - Using motion planning as a primitive in more complex decision making algorithms (task planning)
  - Planning in the presence of multiple agents with uncertainty